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ESE-2019 : MAINS TEST SERIES

UPSC ENGINEERING SERVICES EXAMINATION

ELECTRONICS & TELECOMMUNICATION ENGG. | Test No. 1

Section A : Digital Circuits [All topics]

Section B : Control Systems [All topics]

Time Allowed : 3 hrs. Maximum Marks: 300

Question Paper Specific Instructions

Please read each of the following instructions carefully before attempting questions:

- Answers must be written only in **ENGLISH.**
- There are **EIGHT** questions divided in **TWO** sections.
- Candidate has to attempt **FIVE** questions in all.
- Question no. **1** and **5** are **compulsory** and out of the remaining **THREE** are to be attempted choosing at least **ONE** question from each section.
- The number of marks carried by a question/part is indicated against it.
- Wherever any assumptions are made for answering a question, they must be clearly indicated. Diagrams/figures, wherever required, shall be drawn in the space provided for answering the question itself.
- Unless otherwise mentioned, symbols and notations carry their usual standard meanings. Attempt of questions shall be counted in sequential order. Unless struck off, attempt of a question shall be counted even if attempted partly. Any page or portion of the page left blank in the Question-cum-Answer Booklet must be clearly struck off.

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Section A : Digital Circuits

Q.1 (a) (i) Each of the following arithmetic operations is correct in atleast one number system. Calculate the minimum non-zero base for which the following operations are true.

1. $\frac{54}{4} = 13$
2. $\sqrt{41} = 5$
3. $\frac{302}{20} = 12.1$
4. $3 \times 11 = 33$

(ii) Calculate the minimum non-zero base of x which satisfies the quadratic equation $x^2 - 11x + 22 = 0$, whose roots are $x = 3$ and $x = 6$.

[8 + 4 marks]

(b) What are sequential circuits? Differentiate between sequential and combinational circuits. Explain different types of sequential circuits.

[12 marks]

(c) Draw a well labelled circuit diagram and explain the working of a four bit excess-3 adder using two 4-bit parallel adder IC's.

[12 marks]

(d) Describe the operation of the counter type Analog to Digital converter. What is the conversion time of it?

[12 marks]

(e) What are the advantages and disadvantages of I^2L logic Gate. Implement NAND and NOR gates using I^2L logic.

[12 marks]

Q.2 (a) Prove the following Boolean expressions, without using *K*-Map.

(i) $AB + A\bar{B}C + B\bar{C} = AC + B\bar{C}$

(ii) $A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$

(iii) $BCD + A\bar{C}\bar{D} + ABD = BCD + A\bar{C}\bar{D} + AB\bar{C}$

[5 + 5 + 5 marks]

(b) A clocked sequential circuit is provided with a single input X and a single output Z. Whenever the input produces a string of pulses 111 or 000, at the end of the sequence it produces an output Z = 1; otherwise Z = 0. Overlapping sequences are allowed to detect.

(i) Obtain the state diagram.

(ii) Obtain the state table.

(iii) Design a sequence detector using D-flip flops.

[25 marks]

(c) What is a ROM circuit? Describe briefly different types of ROMs.

[10 marks]

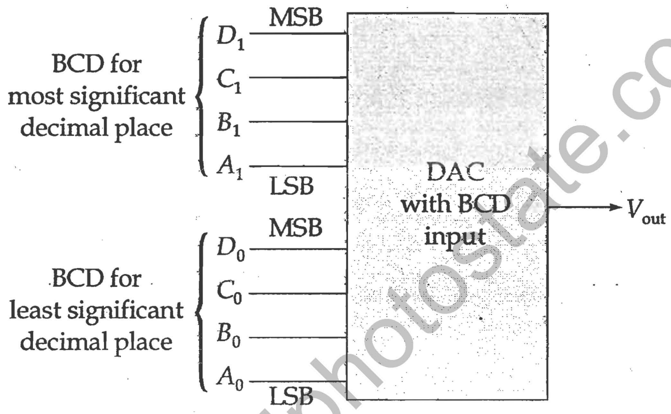
(d) Write the differences between synchronous and asynchronous counters.

[10 marks]

Q.3 (a) Design a 4-bit self-correcting ring counter using D-FF. Also prove that the counter is self-starting and draw a complete state diagram showing all the possible states.

[25 marks]

(b) A DAC uses BCD input code ($D_1C_1B_1A_1\ D_0C_0B_0A_0$) to produce an output ranging from 00 to 99 as shown in the figure below.



If the weight of A_0 is 0.2 V, then find

(i) Step size

(ii) Full-scale output

(iii) Percentage resolution

(iv) The value of output for input BCD code 01100100.

[10 marks]

(c) Consider the following table regarding CMOS and TTL digital logic.

Parameter	CMOS	TTL
$I_{IH(max)}$	1 μA	20 μA
$I_{IL(max)}$	1 μA	0.5 mA
$I_{OH(max)}$	8 mA	2 mA
$I_{OL(max)}$	8 mA	20 mA

Calculate fan-out of the interfacing if

(i) CMOS is used to drive TTL logic.

(ii) TTL is used to drive CMOS logic.

[15 marks]

(d) What do you understand by the term triggering of a flip-flop? What are different types of triggering mechanisms employed to trigger the flip-flop? Design a circuit that will enable a flip-flop to be an edge triggered flip-flop.

[10 marks]

Q.4 (a) (i) Define the following characteristics of a digital-to-analog converter:

1. Resolution
2. Linearity
3. Accuracy
4. Settling time
5. Temperature sensitivity

(ii) If the full scale output of a 10-bit DAC is 5 V, then calculate the resolution and percentage resolution of the DAC.

[15 + 5 marks]

(b) Implement $F(A, B, C) = \Sigma m(0, 2, 4, 7)$ using a 4×1 MUX:

(i) When A and B are connected to select lines.

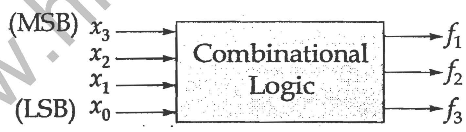
(ii) When A and C are connected to select lines.

(iii) When B and C are connected to select lines.

(iv) Implement the function $F(A, B, C)$ using a 2×1 MUX.

[20 marks]

(c) Consider a multiple input multiple output circuit shown in the figure below:



The output functions are represented as

$f_1(x_3, x_2, x_1, x_0) = \Sigma m(1, 2, 3, 5, 7, 8, 9) + d(12, 14)$

$f_2(x_3, x_2, x_1, x_0) = \Sigma m(0, 1, 2, 3, 4, 6, 8, 9) + d(10, 11)$

$f_3(x_3, x_2, x_1, x_0) = \Sigma m(1, 3, 5, 7, 8, 9, 12, 13) + d(14, 15)$

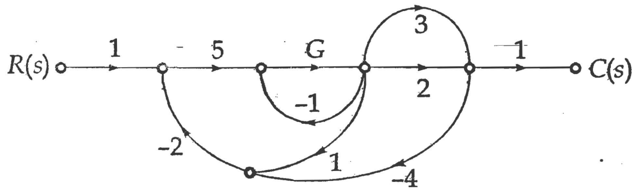
(i) Find the minimal expression of the Boolean functions f_1, f_2 and f_3 using K-map.

(ii) Find the minimal expression for $f(x_3, x_2, x_1, x_0) = f_1 \cdot f_2 \cdot f_3$.

[15 + 5 marks]

Section B : Control Systems

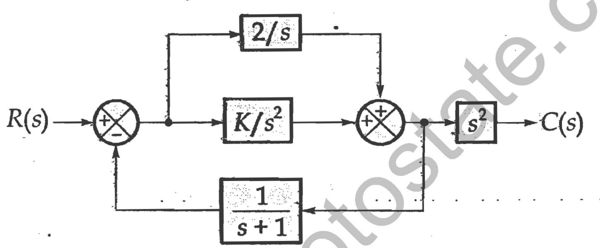
Q.5 (a) Consider the signal flow graph shown below:



Determine the value of gain G if the overall transfer function is given by $\frac{13}{15}$.

[12 marks]

(b) A negative feedback control system is shown in the figure below. Find the range of the system gain 'K' for this system to be stable.

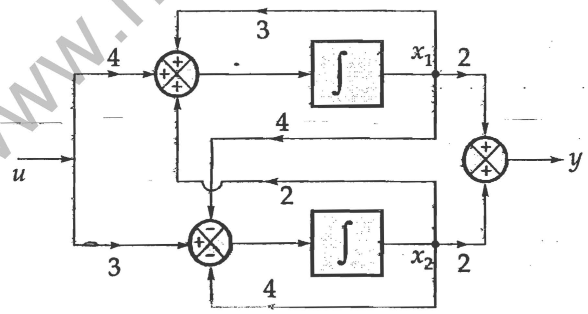


[12 marks]

(c) For the block diagram shown below, find

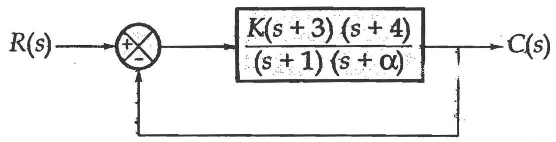
(i) The state space equations of the system.

(ii) Comment on the controllability and observability of the system using Kalman's test.



[6 + 6 marks]

(d) Consider the unity feedback control system shown in the figure below:



If the point $s = -2 + j3$ lies on the root locus of this system, then find the value of α.

[12 marks]

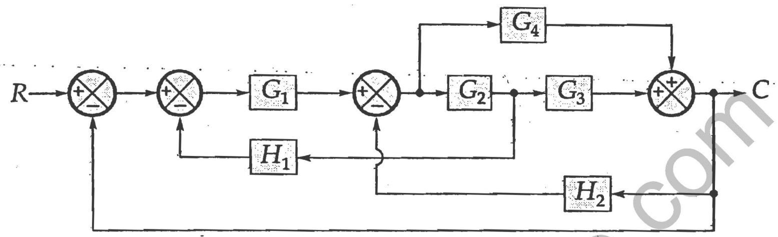
(e) The transfer function of a controller is given by,

$$G_c(s) = \frac{10s+4}{s}$$

If this controller is realised using an operational amplifier, then find the other parameters of the controller with capacitor value of 25 μF.

[12 marks]

Q.6 (a) Consider the block diagram shown in the figure below:



(i) Obtain the transfer function $\frac{C}{R}$ using block diagram reduction technique.

(ii) Verify the result obtained in part (i) using the equivalent signal flow graph and Mason's gain formula.

[12 + 8 marks]

(b) A unity negative feedback control system has an open loop transfer function $G(s) = \frac{10}{s(s+2)}$. Find:

(i) The unit step response.
(ii) The natural frequency of oscillation and damping ratio.
(iii) Maximum peak overshoot and the peak time.
(iv) Steady state error to an input $(1 + 4t)u(t)$.
(v) For this system, if two pole are introduced in the open loop at $\pm\sqrt{5}j$, then comment on the stability of the new closed loop system.

[20 marks]

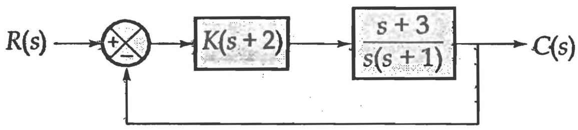
(c) The closed-loop transfer function of a system is given by,

$$\frac{C(s)}{R(s)} = \frac{5(s+1)}{s^2+2s+5}$$

Find the unit step response, the peak time and the percentage maximum peak overshoot of the unit step response.

[20 marks]

Q.7 (a) For a control system shown in the figure below, draw the root locus diagram neatly by showing all the relevant calculations. From the diagram comment on how the value of K will make the system underdamped or overdamped.



[20 marks]

(b) The open loop transfer function of a system with unity negative feedback is given by,

$$G(s)=\frac{K(s+4)}{s(s+1)(s+2)}$$

Using Routh's stability criteria, find

(i) The range of K that keeps the system stable.

(ii) The frequency of oscillation when K is set to the value that makes the system oscillate.

(iii) For $K = 1$, check if all the poles of the closed loop transfer function produce critically damped response.

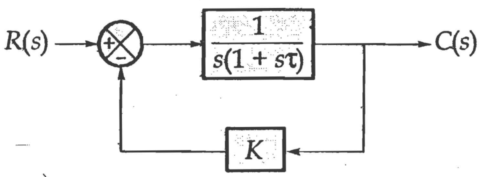
[6 + 6 + 8 marks]

(c) Determine the value of T for stability limit of a unity feedback control system having open loop transfer function,

$$G(s)=e^{-sT}\frac{10}{s(0.1s+1)}$$

using Nyquist criteria. **[20 marks]**

Q.8 (a) For the feedback control system shown in the figure below, determine the parameter K and τ such that the following time domain specifications get satisfied.



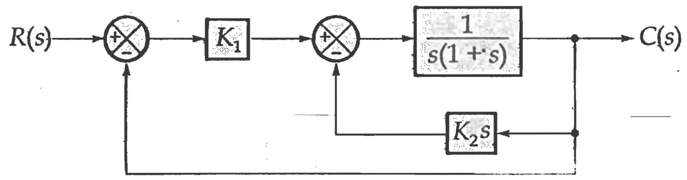
(i) The percentage peak overshoot $M_p = 5\%$.

(ii) The peak time $\tau_p = 2$ sec.

(iii) The steady state output of the system is 0.5, for $r(t) = 10u(t)$.

[20 marks]

(b) Consider the feedback control system shown below.



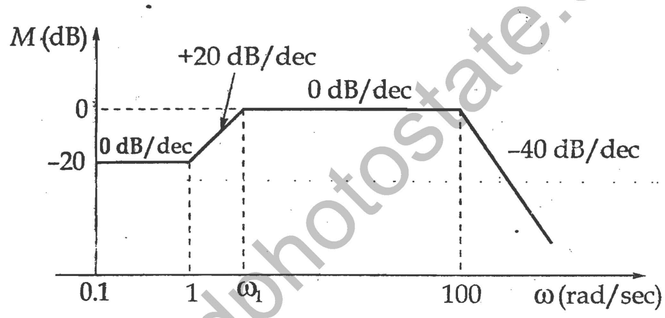
If the frequency domain specifications are given as $M_r = 1.41$ and $\omega_r = 9$ rad/sec, then find

(i) the value of K_1 and K_2.

(ii) the expression for closed loop transfer function.

[12 + 8 marks]

(c) (i) Obtain the open loop transfer function for a system with unity feedback whose bode plot is shown below.



(ii) A unity negative feedback control system has forward path transfer function,

$$G(s) = \frac{K(2s+1)}{s(5s+1)(s+1)^2}$$

If the input $r(t) = (1 + 6t)u(t)$ is applied to the system, then determine the minimum value of K such that the steady state error will be less than 0.5.

[12 + 8 marks]

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ESE-2019 Mains Test Series

E & T Engineering Test No : 1

Section A : Digital Circuits

Q.1 (a) Solution:

(i)

1. Let the base of the expression be 'x'.

thus,
$$\frac{(54)_x}{(4)_x} = (13)_x$$
$$\Rightarrow \quad \frac{5x+4}{4} = x + 3$$
$$\Rightarrow \quad 5x + 4 = 4x + 12$$
$$x = 8$$

Hence, the minimum non-zero base is equal to '8'.

2. Let the base of the expression be equal to 'x'.
$$\sqrt{(41)_x} = (5)_x$$
$$\sqrt{4x+1} = 5$$
$$4x + 1 = 25$$
$$x = 6$$

Hence, the minimum non-zero base for the expression is equal to 6.

3. Let the base of the expression be equal to x.
$$\frac{(302)_x}{(20)_x} = (12.1)_x$$

$$\frac{3x^2+2}{2x} = x+2+\frac{1}{x}$$

$$\frac{3x^2+2}{2} = x^2 + 2x + 1$$

$$x^2 - 4x = 0$$

$$x = 0, 4$$

Thus, the non-zero base is equal to 4.

4. Let the base of the expression be equal to 'x'.

$$(3)_x \times (11)_x = (33)_x$$

$$3(x + 1) = 3x + 3$$

$$3x + 3 = 3x + 3$$

Thus, the equation is valid for any value of x. So the minimum non-zero base will be equal to $x = 4$.

(ii)

The given quadratic equation,

$$x^2 - 11x + 22 = 0 \quad \text{...(i)}$$

The factor of solution are 3 and 6.

Thus, the equation can also be written as

$$x^2 - (\alpha + \beta)x + \alpha\beta = 0$$

$$x^2 - [(3)_b + (6)_b]x + (3)_b \times (6)_b = 0 \quad \text{...(ii)}$$

Equating equation (i) and (ii), we get,

$$(3)_b + (6)_b = (11)_b$$

and $$(3)_b \times (6)_b = (22)_b$$

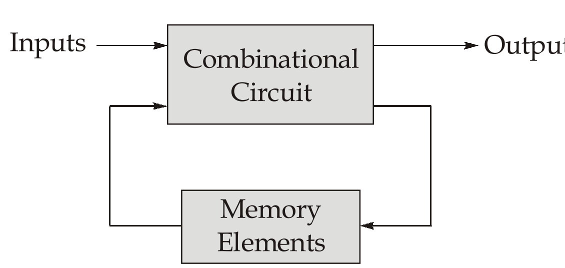
$$3 + 6 = b + 1$$

$\therefore$ $$b = 8$$

$\therefore$ The minimum non-zero base = 8.

Q.1 (b) Solution:

Sequential circuits are those whose output levels at any instance of time depend not only on the level present at the input at that time, but also on the state of circuit i.e., on the prior input level condition (past value). In other words, they are combinational circuits with memory.



The difference between sequential and combinational circuit can be summarized below:

Combinational Circuits	Sequential Circuits
1. The output variables at any instant of time depends only on the present input variables.	1. The output variables at any instant of time depends not only on the present input variables but also on the past history of the system.
2. These circuits do not require any memory element, hence called memory less system.	2. To store the past history of the input variables, memory unit is required.
3. Combinational circuits are faster.	3. Sequential circuits are slower.
4. They are easy to design.	4. They are comparatively harder to design.

The sequential circuits are classified as synchronous sequential circuits and asynchronous sequential circuits depending on the timing of their signals.

(i) Synchronous Sequential Circuit

- The change in input signals can affect memory element upon activation of clock signals.
- The maximum operational speed of clock depends on time delays involved.
- In this circuit, memory elements are "clocked flip-flops".
- It is easier to design.
- It is generally "edge triggered".

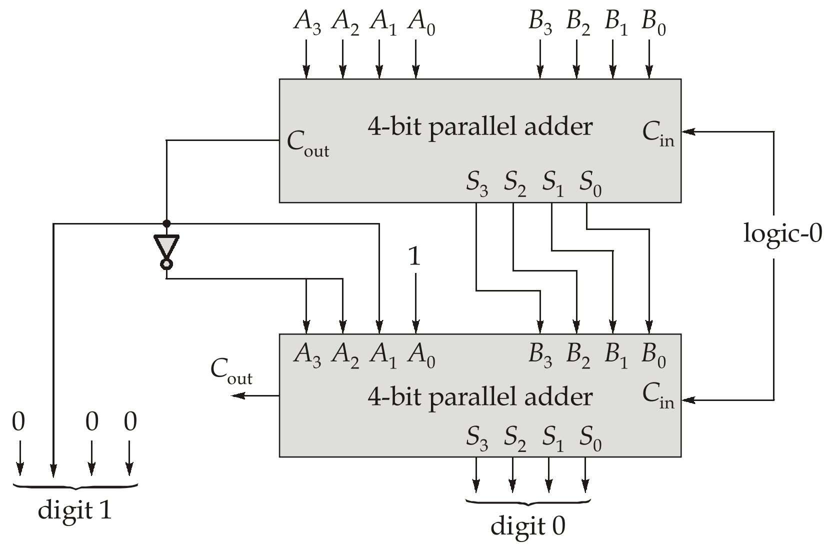
(ii) Asynchronous Sequential Circuit

- The change in input signals can affect memory element at any instant of time.
- Because of absence of clock, this circuit can operate faster than synchronous circuit.
- In this circuit, memory elements are either "unclocked flip-flops" or time delay elements.
- More difficult to design.
- It is generally "Level triggered".

Q.1 (c) Solution:

To perform Excess-3 addition, we will have to

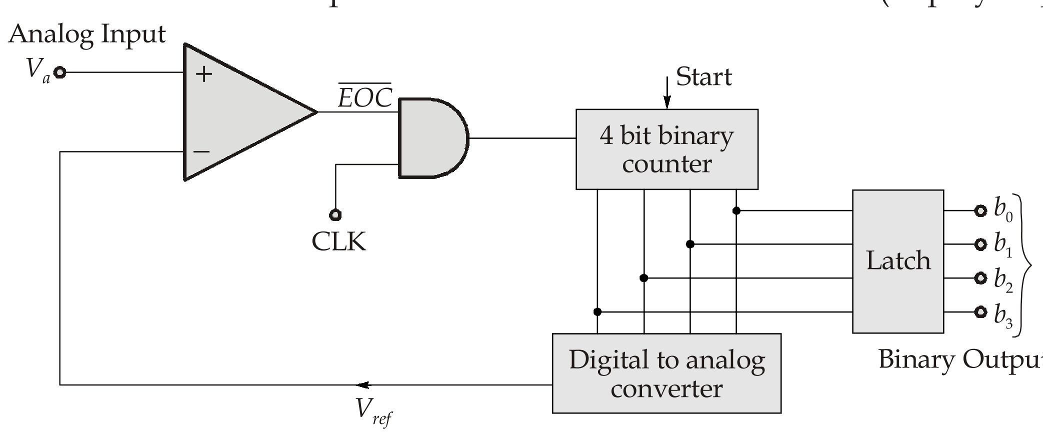
1. Add two Excess-3 numbers.
2. If a carry is generated, then we will add 3(0011) to the sum of those two code group.
3. If carry is not generated, then subtract 3(0011), from the sum or add 1101(13) to the sum of two codes.



The augend ($A_3A_2A_1A_0$) and addent ($B_3B_2B_1B_0$) in excess-3 added up using the 4-bit parallel adder. If the carry is 1, then 3(0011) is added to the sum bits $S_3S_2S_1S_0$ of the upper adder in the lower 4-bit parallel adder. If the carry is 0, then (13) (1101) is added to the sum bit which is equivalent of subtracting 3(0011) to from the sum bit.

Q.1 (d) Solution

- It is the simplest type of ADC which employs a binary counter, an analog comparator, a control circuit (an AND gate) and a DAC as shown below.
- The counter type A/D converter is also known as a digital ramp ADC, because the waveform at the output of the DAC is a staircase waveform (step-by-step ramp).



Operation

- In a counter type ADC the analog voltage (V_a) which is to be converted is applied to the non-inverting terminal of the comparator. The output from the DAC (V_{ref}) is applied to the inverting terminal of the Op-Amp.
- The counter is used to count the number of clock pulses applied. A start pulse is applied to reset the counter to zero. Initially $V_{ref} = 0\ V$.

- Whenever the analog input signal is greater than the reference voltage provided by DAC, the output of the comparator become HIGH (logic 1), the AND gate is enabled and, so, the clock pulses are transmitted to the counter.
- If the analog voltage $V_a < V_{ref}$, then the comparator output become LOW (logic 0) and the counter will stop counting. At this time the output of the counter will provide the digital output proportional to the analog input. The control logic loads the binary count into the latches and resets the counter, thus beginning another count sequence to sample the input value. The cycle thus repeats itself.

Conversion Time

The conversion time is the time interval between the starting of the conversion and the time the comparator output is LOW (stopping the count).

$$t_{c\,(max)} = (2^N - 1) \times t_{CLK}$$

$$\text{Average conversion time} = \frac{t_{c(max)}}{2}$$

where, N = Number of bits in the counter.

Thus, the maximum number of clock pulses required for N-bit conversion is $(2^N - 1)$.

Q.1 (e) Solution

Advantages of I^2L

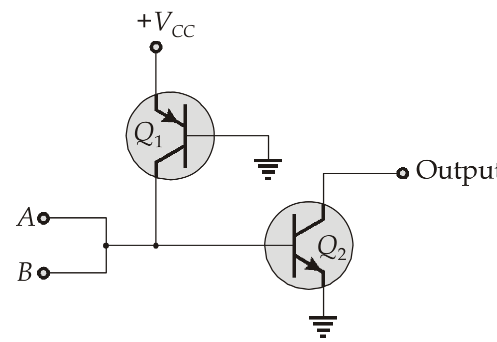
1. I^2L gates have high speed of operation because they are made up of BJTs.
2. Because only transistors are used for construction, I^2L gates have high packing density, and are hence suitable for the construction of VLSI circuits.
3. Very low power-supply requirement.
4. Low power dissipation.
5. Process-steps required are less. Hence cost per gate is low.
6. Several functions possible on the same chip.
7. Using standard bipolar technology, it is possible to combine I^2L logic with other logic families.

Disadvantages of I^2L

1. Very low power-supply requirement.
2. Lower packing density than NMOS.
3. Lower noise margin.
4. External resistance required for proper functioning.
5. I^2L technology, at present, is dormant.

I^2L NAND Gate

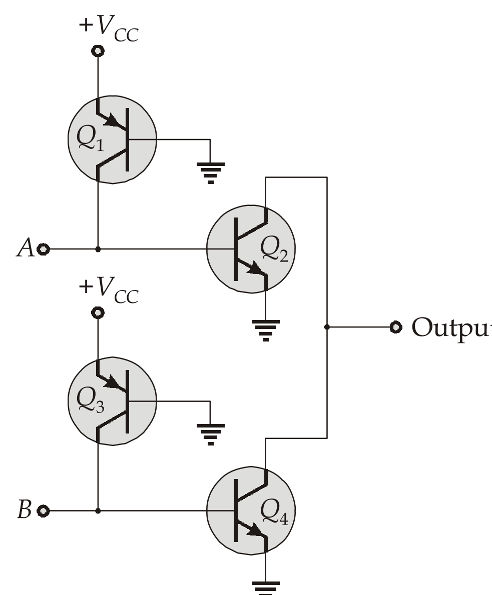
The I^2L NAND gate shown in figure below is simply an inverter with inputs connected directly together at the inverter input. If, either input A, or input B, or both the inputs A and B are LOW (current sinks), the injected current flows into those inputs and Q_2 remains OFF (HIGH). If both the inputs are HIGH, the injected current turns on Q_2 making the output LOW. Thus, the NAND operation is performed. The transistor Q_1 is called a current injector transistor, because when its emitter is connected to an external power sources, it can supply current to the base of Q_2.



Two-input I^2L NAND gate

I^2L NOR Gate

The I^2L NOR gate shown in figure below is simply two inverters with their outputs connected together. If either or both the inputs are HIGH, the corresponding output transistor is ON and the output is a current sink. So, the output is LOW. If both the inputs are LOW, both the output transistors are OFF, and so, the output is HIGH. This is a NOR operation.



Two-input I^2L NOR gate

Q.2 (a) Solution:

(i)

$$\begin{aligned} AB + A\bar{B}C + B\bar{C} &= A(B+\bar{B}C) + B\bar{C} \\ &= A(B+\bar{B})(B+C) + B\bar{C} \\ &= AB + AC + B\bar{C} = AB(C+\bar{C}) + AC + B\bar{C} \\ &= ABC + AB\bar{C} + AC + B\bar{C} = AC(1+B) + B\bar{C}(1+A) \\ &= AC + B\bar{C} \end{aligned}$$

(ii)

$$\begin{aligned} A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C &= A\bar{B}C + \bar{A}C + B(1+\bar{D}+A\bar{D}) \\ &= C(\bar{A}+A\bar{B}) + B = C(\bar{A}+A)(\bar{A}+\bar{B}) + B \\ &= C\bar{A} + C\bar{B} + B = (B+C)(B+\bar{B}) + C\bar{A} \\ &= B + C + C\bar{A} = B + C(1+\bar{A}) \\ &= B + C \end{aligned}$$

(iii)

$$BCD + A\bar{C}\bar{D} + ABD = BCD + A\bar{C}\bar{D} + (ABD)\cdot(C+\bar{C})$$

$$= BCD + A\bar{C}\bar{D} + ABDC + AB\bar{C}D$$

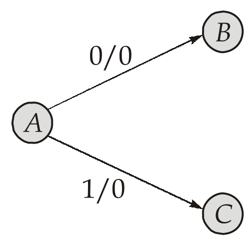
$$= BCD(1+A) + A\bar{C}(\bar{D} + DB) = BCD + A\bar{C}(\bar{D}+B)$$

$$= BCD + A\bar{C}\bar{D} + AB\bar{C}$$

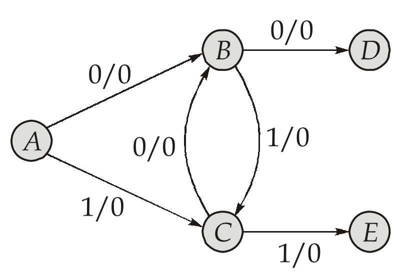
Q.2 (b) Solution:

Let the initial state of machine be A, now from this state, there will be two branches, one will detect the sequence 000 and the other will detect a sequence of 111.

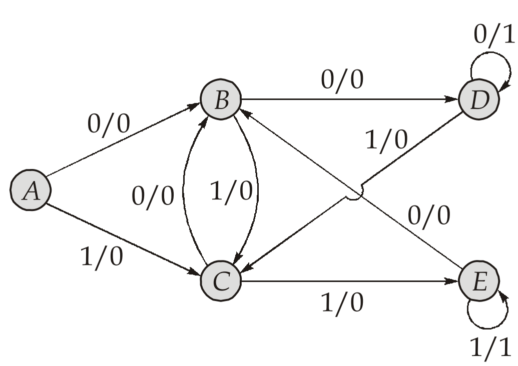
Now, from state A, the machine will go to state B if it receives 0 and will go to state C if it receives 1.



Now, the state will change from B to D if another 0 is received, the state will change from C to E if another 1 is received. But if state B receives a 1 or state C receives a zero, then the states will interchange.



Since repetition is allowed, state D will keep producing output 1 till it receives input as 0 or else it will go to state C. Similarly state E will keep producing output 1 till it receives input as 1 or else it will go to state B.



∴ State table

Present State	Next state		Output (Z)	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
A	B	C	0	0
B	D	C	0	0
C	B	E	0	0
D	D	C	1	0
E	B	E	0	1

Now, since no reduction is possible, thus we can assign state

A - 000
B - 001
C - 010
D - 011
E - 100

∴ The transition table can be drawn as

Present State $Q_1Q_2Q_3$	Next state		Output (Z)	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
000	001	010	0	0
001	011	010	0	0
010	001	100	0	0
011	011	010	1	0
100	001	100	0	1

Now, to implement the circuit we will have to write the excitation table.

Present state			Input	Next state			Excitations			Output
Q_1	Q_2	Q_3	X	Q_1^+	Q_2^+	Q_3^+	D_1	D_2	D_3	Z
0	0	0	0	0	0	1	0	0	1	0
0	0	0	1	0	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1	0
0	0	1	1	0	1	0	0	1	0	0
0	1	0	0	0	0	1	0	0	1	0
0	1	0	1	1	0	0	1	0	0	0
0	1	1	0	0	1	1	0	1	1	1
0	1	1	1	0	1	0	0	1	0	0
1	0	0	0	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1	0	0	1
1	0	1	0	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x

Q_1Q_2 \ Q_3X	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	x	x	x	x
10	0	1	x	x

$D_1 = Q_1X + Q_2\bar{Q}_3X$

Q_1Q_2 \ Q_3X	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	x	x	x	x
10	0	0	x	x

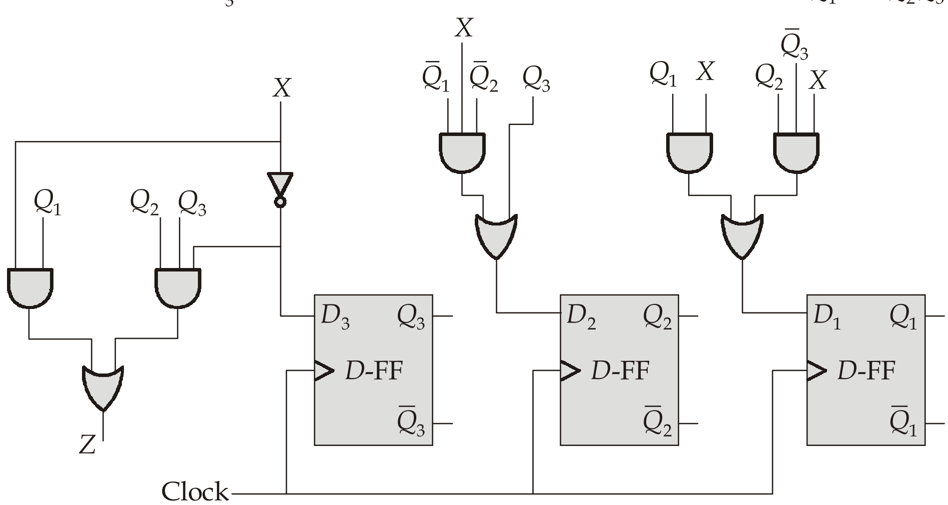
$D_2 = \bar{Q}_1\bar{Q}_2X + Q_3$

Q_1Q_2 \ Q_3X	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	x	x	x	x
10	1	0	x	x

$D_3 = \bar{X}$

Q_1Q_2 \ Q_3X	00	01	11	10
00	0	0	0	0
01	0	0	0	1
11	x	x	x	x
10	0	1	x	x

$Z = Q_1X + Q_2Q_3\bar{X}$



Q.2 (c) Solution:

A Read-only memory (ROM) is essentially a memory device in which permanent binary information is stored. The binary pattern is specified by the designer and it is then embedded in the unit to form the required inter-connected pattern.

Types of ROM:

1. **Mask Programmable read-only memory**

   This type of memory is referred to as ROM only. Once it is programmed the data pattern cannot be changed.

2. Programmable read-only memory (PROM)

This type of memory comes from the manufacturer without any data stored in it. The data pattern is programmed electrically by the user.

3. Erasable Programmable read-only memory (EPROM)

In this type of memory, data can be written any number of times, they are reprogrammable. The content already stored are easily erased by exposing UV light.

4. Electrically Erasable Programmable read-only memory

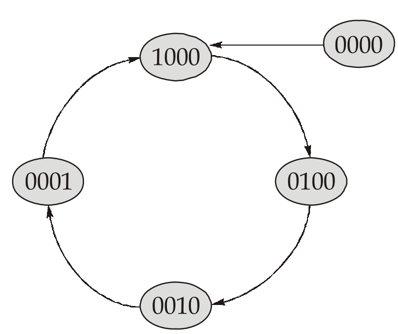
In this type of memory data can be stored any number of times and is erased using electric charge.

Q.2 (d) Solution

Asynchronous Counter	Synchronous Counter
1. All the flip-flops are not clocked simultaneously.	1. All the flip-flops are clocked simultaneously.
2. Output of one flip-flop is used to generate clock for the another flip-flop.	2. There is no connection between the output of one flip-flop and the clock of the another flip-flop.
3. Only fixed sequence of states can be designed by using these counters.	3. Any required sequence of states can be designed by using these counters.
4. Design and implementation is very simple even for more number of states (if they are in proper sequence).	4. Design and implementation become tedious and complex as the number of states increases.
5. Operation is slower as the clock must be propagated through all the flip-flops before reaching the last flip-flop.	5. Operation is faster, as all the flip-flops get the clock simultaneously.
6. Decoding errors will occur.	6. No decoding errors will occur.
7. e.g. Ripple up counter, Ripple down counter	7. e.g. Ring counter, Johnson counter.

Q.3 (a) Solution:

Assume that the ring counter is initially cleared to '0000', thus the state diagram for 4-bit ring counter can be drawn as



Now, the state excitation table can be drawn as,

Present State				Next State				Excitation Table			
Q_A	Q_B	Q_C	Q_D	Q_A^+	Q_B^+	Q_C^+	Q_D^+	D_A	D_B	D_C	D_D
0	0	0	0	1	0	0	0	1	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0
0	0	1	0	0	0	0	1	0	0	0	1
0	0	1	1	x	x	x	x	x	x	x	x
0	1	0	0	0	0	1	0	0	0	1	0
0	1	0	1	x	x	x	x	x	x	x	x
0	1	1	0	x	x	x	x	x	x	x	x
0	1	1	1	x	x	x	x	x	x	x	x
1	0	0	0	0	1	0	0	0	1	0	0
1	0	0	1	x	x	x	x	x	x	x	x
1	0	1	0	x	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x	x

Thus, from excitation table, we get,

Q_CQ_D \ Q_AQ_B	00	01	11	10
00	1	0	x	0
01	1	x	x	x
11	x	x	x	x
10	0	x	x	x

$D_A = \bar{Q}_A\bar{Q}_B\bar{Q}_C$

Q_CQ_D \ Q_AQ_B	00	01	11	10
00	0	0	x	1
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

$D_B = Q_A$

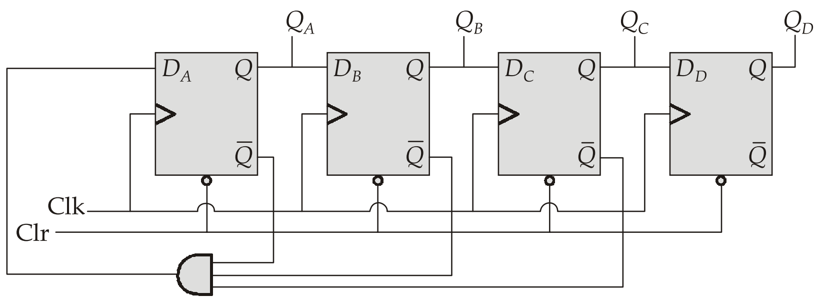
Q_CQ_D \ Q_AQ_B	00	01	11	10
00	0	1	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

$D_C = Q_B$

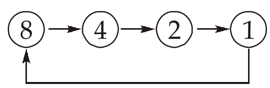
Q_CQ_D \ Q_AQ_B	00	01	11	10
00	0	0	x	0
01	0	x	x	x
11	x	x	x	x
10	1	x	x	x

$D_D = Q_C$

Logic circuit implementation,



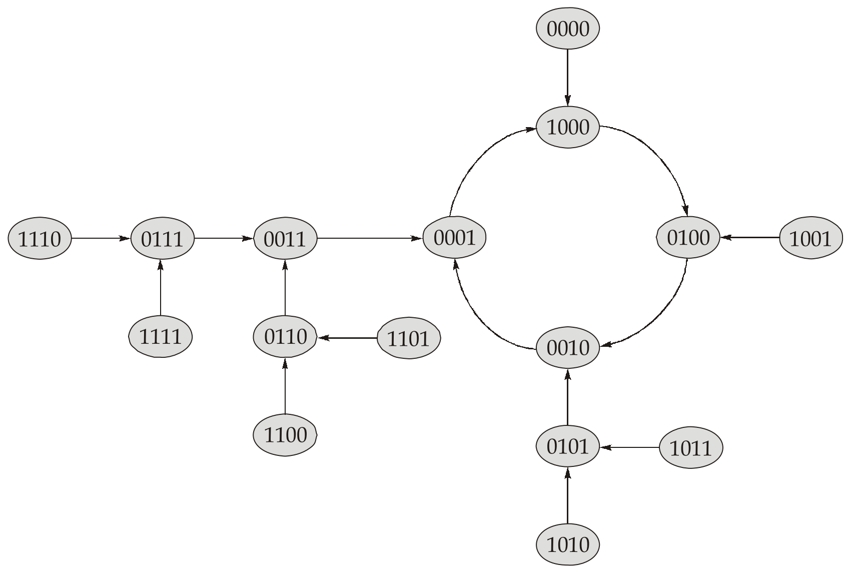
States considered =



Now, to prove the counter is self-starting we have to check the rest of states.

	Present State				Next State				
					Q_A^+	Q_B^+	Q_C^+	Q_D^+	
	Q_A	Q_B	Q_C	Q_D	$\bar{Q}_A\bar{Q}_B\bar{Q}_C$	Q_A	Q_B	Q_C	
14	1	1	1	0	0	1	1	1	
	0	1	1	1	0	0	1	1	
	0	0	1	1	0	0	0	1	→ Valid State
15	1	1	1	1	0	1	1	1	
	0	1	1	1	0	0	1	1	
	0	0	1	1	0	0	0	1	→ Valid State
13	1	1	0	1	0	1	1	0	
	0	1	1	0	0	0	1	1	
	0	0	1	1	0	0	0	1	→ Valid State
12	1	1	0	0	0	1	1	0	
	0	1	1	0	0	0	1	1	
	0	0	1	1	0	0	0	1	→ Valid State
11	1	0	1	1	0	1	0	1	
	0	1	0	1	0	0	1	0	→ Valid State
10	1	0	1	0	0	1	0	1	
	0	1	0	1	0	0	1	0	→ Valid State
9	1	0	0	1	0	1	0	0	→ Valid State
7	0	1	1	1	0	0	1	1	
	0	0	1	1	0	0	0	1	→ Valid State
6	0	1	1	0	0	0	1	1	
	0	0	1	1	0	0	0	1	→ Valid State
5	0	1	0	1	0	0	1	0	→ Valid State
3	0	0	1	1	0	0	0	1	→ Valid State
0	0	0	0	0	1	0	0	0	→ Valid State

Thus combined state diagram can be constructed as follows:



Thus, the counter is self-starting.

Q.3 (b) Solution:

(i) Step size is equal to the change in the output for minimum change in input. Thus, weight of A_0 will be equal to the step size of the circuit.

$$\therefore \quad \text{Step size} = 0.2 \text{ V}$$

(ii) Since there are 99 steps, thus the full scale output voltage is equal to

$$V_{FS} = 99 \times 0.2 = 19.8 \text{ V}$$

(iii) Thus, the percentage resolution can be given as

$$= \frac{\text{Step size}}{\text{Full scale output}} \times 100 = \frac{0.2}{19.8} \times 100 = 1.01\%$$

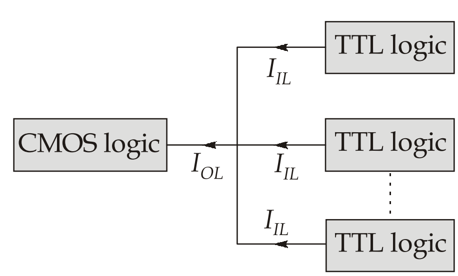
(iv) The output of the number can be represented as

$$V_{out} = k[\text{Decimal equivalent}] = 0.2 \times (64)_{10} = 12.8 \text{ V}$$

Q.3 (c) Solution:

(i) CMOS is used to drive TTL logic

To determine low state fan-out.



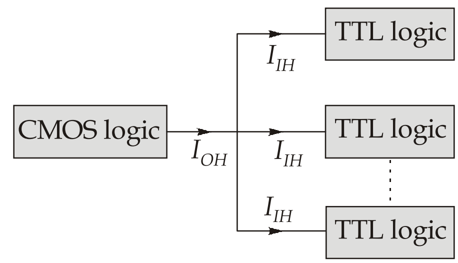
$$\therefore \quad nI_{IL} \le I_{OL}$$

$$n \le \frac{I_{OL}}{I_{IL}}$$

$$\therefore \quad n \le \frac{8 \times 10^{-3}}{0.5 \times 10^{-3}}$$

$$n \le 16$$

To determine high state fan-out



$$nI_{IH} \leq I_{OH}$$

$$n \leq \frac{I_{OH}}{I_{IH}}$$

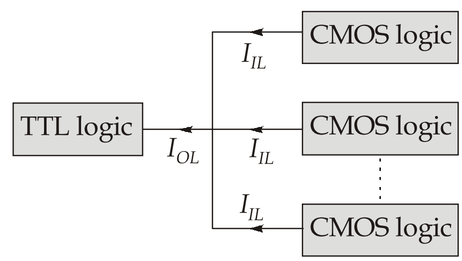
$$\therefore \quad n \leq \frac{8\times10^{-3}}{20\times10^{-6}}$$

$$n \leq 400$$

$$\therefore \quad \text{fan-out} = \min\{16, 400\} = 16$$

(ii) TTL is used to drive CMOS logic.

To determine low state fan-out.



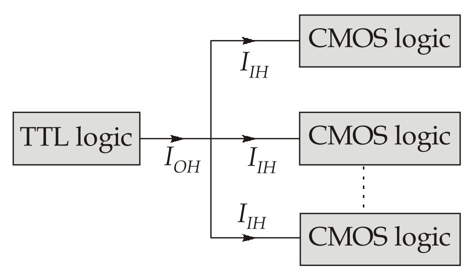
$$nI_{IL} \leq I_{OL}$$

$$n \leq \frac{I_{OL}}{I_{IL}}$$

$$n \leq \frac{20\times10^{-3}}{1\times10^{-6}}$$

$$n \leq 20000$$

To determine high state fan-out



$$nI_{IH} \leq I_{OH}$$

$$n \leq \frac{I_{OH}}{I_{IH}}$$

$$n \leq \frac{2\times10^{-3}}{1\times10^{-6}} = 2000$$

$$\therefore \quad \text{fan-out} = \min\{20000, 2000\} = 2000$$

Q.3 (d) Solution:

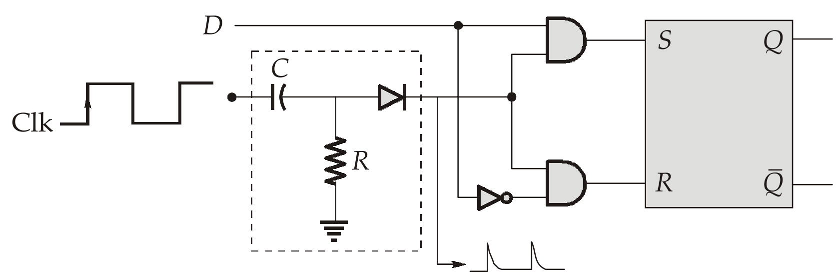
Flip-flops are synchronous bistable devices. To change the output at a specific point of time is termed as triggering of a flip-flop. Based on specific interval or point in clock duration which acts as input trigger to the circuit, it is classified into two different types.

(i) Level triggering :- The flip-flop changes its state when the clock is positive (in case of positive level triggered) and negative (in case of negative level triggered).

(ii) Edge triggered flip-flop: A clock pulse goes through two signal transactions from 0 to 1 and returns from 1 to 0. A pulse transition from 1 to 0 is defined as a negative edge. A pulse transition from 0 to 1 is defined as a positive edge. Thus edge triggering means that the flip-flop either changes its state either at positive edge (rising or leading edge) or at negative edge (falling or trailing edge) of the clock pulse.

Circuit Diagram

One way to make a flip-flop respond only to a pulse transition is to use capacitive coupling. The R.C. circuit can be used to generate a spike at the positive/negative edge and to make a flip-flop respond to momentary change in the input signal.

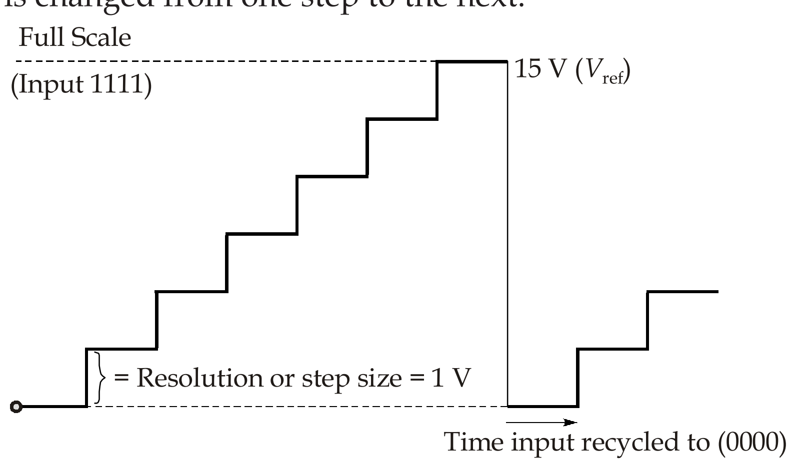


Q.4 (a) Solution:

(i)

Resolution

- The resolution of a DAC is defined as the smallest possible change in output voltage corresponding to the change in the digital input signal.
- The resolution is always equal to the "weight of the LSB" and is also referred to as the "step size", since it is the amount that V_0 will change as the digital input value is changed from one step to the next.



Linearity

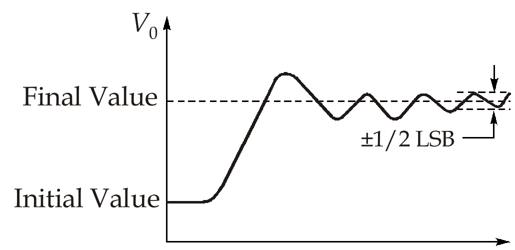
The linearity of a converter is a measure of the precision with which the linear input-output relationship is satisfied. In an ideal DAC, equal increments in the numerical significance of the digital-input should yield equal increments in the analog output. The linearity of a converter serves as a measure of the precision with which this requirement is satisfied. The "linearity" of a converter depends principally on the accuracy of the resistors. Also, the linearity may be adversely affected by substantial temperature changes.

Accuracy

It is a measure of the difference between actual analog output voltage and what the output should be in the ideal case. Also, it is the maximum deviation of DAC output from its expected value. It is specified as a "% of full scale voltage (FSV)". Lack of linearity contributes to inaccuracy.

Settling Time

When the digital input to D/A converter changes, the analog output voltage does not change abruptly. Because of the presence of switches, active devices, stray capacitance, and inductance associated with the passive circuit components, the transients appear in the output voltage and oscillations may also occur. The time required for the analog output to settle to within ±1/2 LSB of the final value after a change in the digital input is usually specified by the manufacturers and is referred to as settling time.



Temperature Sensitivity

At any fixed digital input, the analog output will vary with temperature, this is referred as "temperature sensitivity". The overall temperature sensitivity is due to the temperature sensitivity of the reference voltages, resistors, OP-AMP and even the amplifier offset voltage. Typical value ranges from about ± 50 ppm/°C to ±1.5 ppm/°C. For a good quality of DAC, it should be minimum.

(ii)

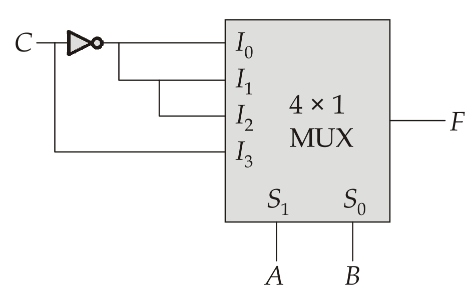
$$\text{Resolution} = \frac{\text{Full scale output}}{2^n - 1} = \frac{5}{2^{10} - 1} = 4.89 \text{ mV}$$

$$\%\text{Resolution} = \frac{1}{2^n - 1} \times 100 = \frac{1}{2^{10} - 1} \times 100 = 0.098\,\%$$

Q.4 (b) Solution:

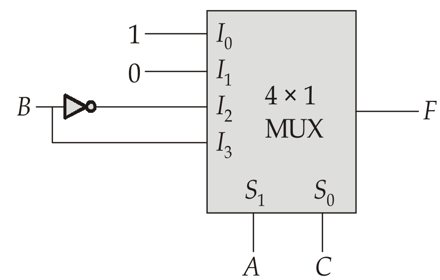
(i) If A and B are connected to the select lines.

Select Line	I_0	I_1	I_2	I_3
AB	00	01	10	11
$\bar{C}$	(0)	(2)	(4)	6
C	1	3	5	(7)
	$\bar{C}$	$\bar{C}$	$\bar{C}$	C



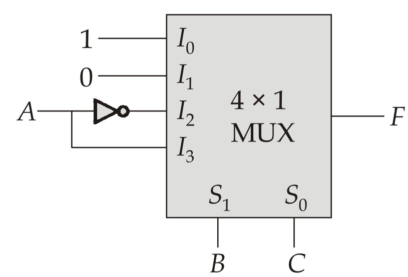
(ii) If A and C are connected to select line

Select Line	I_0	I_1	I_2	I_3
AC	00	01	10	11
$\bar{B}$	(0)	1	(4)	5
B	(2)	3	6	(7)
	1	0	$\bar{B}$	B

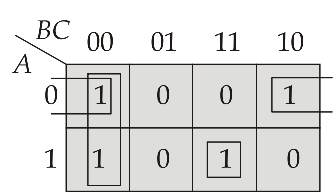


(iii) If B and C are select lines

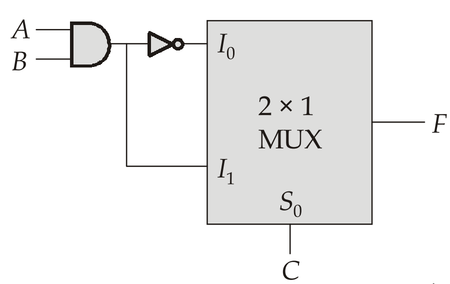
Select Line	I_0	I_1	I_2	I_3
BC	00	01	10	11
$\bar{A}$	(0)	1	(2)	3
A	(4)	5	6	(7)
	1	0	$\bar{A}$	A



(iv) Now drawing K-map of the above function, we get,

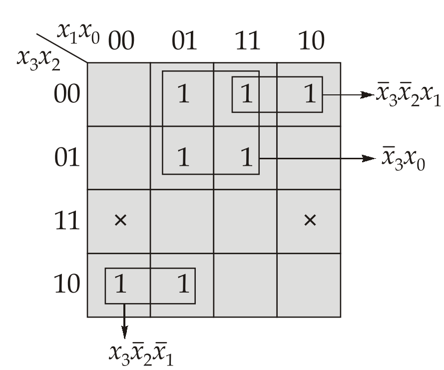


$\therefore$ $$f(A, B, C) = \Sigma m(0, 2, 4, 7) = ABC + \bar{B}\bar{C} + \bar{A}\bar{C} = \bar{C}(\overline{AB}) + C(AB)$$



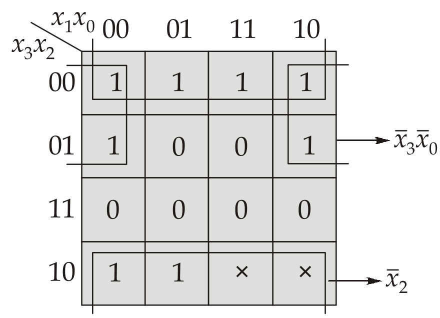
Q.4 (c) Solution:

(i) The minimised Boolean expression for the function f_1 can be obtained by drawing K-map of the function.



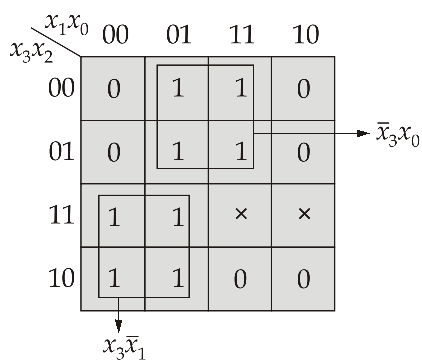
$\therefore$ $$f_1(x_3, x_2, x_1, x_0) = x_3\bar{x}_2\bar{x}_1 + \bar{x}_3\bar{x}_2x_1 + \bar{x}_3x_0$$

Drawing K-map for function f_2, we get,



Therefore, $f_2(x_3, x_2, x_1, x_0) = \bar{x}_2 + \bar{x}_3\bar{x}_0$

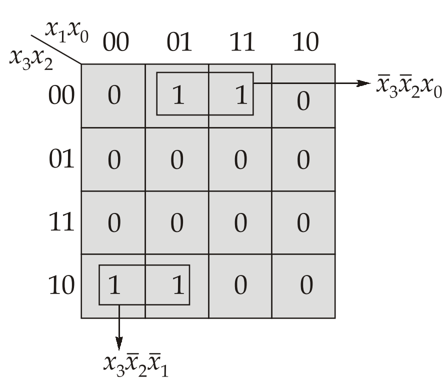
Drawing K-map for function f_3, we get,



Therefore, $f_3(x_3, x_2, x_1, x_0) = \bar{x}_3x_0 + x_3\bar{x}_1$

(ii) For the function,

$$f(x_3\, x_2\, x_1\, x_0) = f_1\, f_2\, f_3 = \Sigma m(1, 3, 8, 9)$$

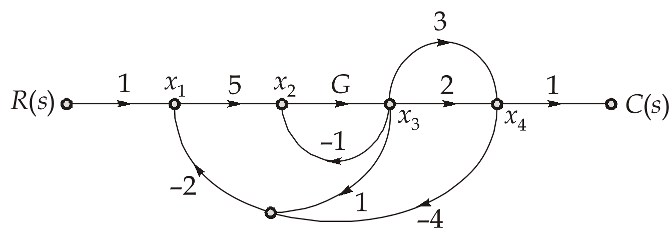


$\therefore$ $f(x_3\, x_2\, x_1\, x_0) = x_3\bar{x}_2\bar{x}_1 + \bar{x}_3\bar{x}_2x_0$

Section B : Control Systems

Q.5 (a) Solution:

The signal flow graph can be redrawn as



Here, the forward paths are,

$$P_1 \Rightarrow R - x_1 - x_2 - x_3 - x_4 - C = 10G$$

and $$P_2 \Rightarrow R - x_1 - x_2 - x_3 - x_4 - C = 15G$$

Also, $$\Delta_1 = \Delta_2 = 1$$

Loops:

$$L_1 = 5 \times G \times 2 \times 4 \times 2 = 80G$$
$$L_2 = -5 \times G \times 2 = -10G$$
$$L_3 = -G$$

and $$L_4 = 5 \times G \times 3 \times 4 \times 2 = 120G$$

∴ Overall gain

$$\frac{C(s)}{R(s)} = \frac{10G + 15G}{1 + 10G - 120G - 80G + G}$$

$$\frac{13}{15} = \frac{25G}{1 - 189G}$$

$$13 - 2457G = 375G$$

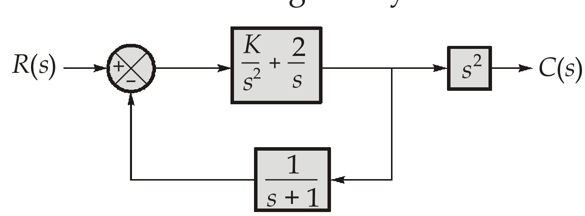
or $$13 = 2832G$$

or $$G = \frac{13}{2832}$$

$$G = 4.59 \times 10^{-3}$$

Q.5 (b) Solution:

The closed loop transfer function of the given system can be calculated as



The parallel loop $\frac{K}{s^2}$ and $\frac{2}{s}$ combinely gives $\left[\frac{K}{s^2}+\frac{2}{s}\right]$, therefore by using feedback formula with $\left(\frac{K}{s^2}+\frac{2}{s}\right)$ and $\left(\frac{1}{s+1}\right)$, we get,

$$\therefore \qquad T'(s) = \frac{\left(\frac{K}{s^2}+\frac{2}{s}\right)}{1+\left(\frac{1}{s+1}\right)\left(\frac{K}{s^2}+\frac{2}{s}\right)}$$

$\therefore$ the complete transfer function is

$$\Rightarrow \qquad T(s) = s^2T'(s) = \frac{2s^4+(K+2)s^3+Ks^2}{s^3+s^2+2s+K}$$

$\therefore$ The characteristic equation becomes $s^3 + s^2 + 2s + K = 0$

Using Routh's criterion, we get,

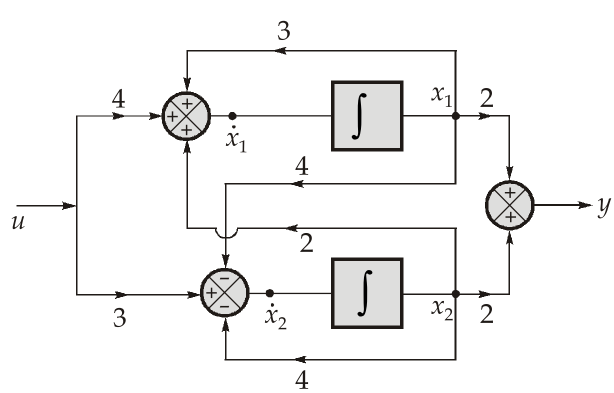
s^3	1	2
s^2	1	K
s^1	$2-K$	
s^0	K	

For system to be stable, $2 - K > 0 \therefore K < 2$

$\therefore$ The range of K is $0 < K < 2$.

Q.5 (c) Solution:

(i) The block diagram is redrawn below as



$\therefore$ The state equations can be written are,

$$y = 2x_1 + 2x_2 \qquad \text{...(i)}$$

$$\dot{x}_1 = 3x_1 + 2x_2 + 4u \quad ...(ii)$$

$$\dot{x}_2 = -4x_1 - 4x_2 + 3u \quad ...(iii)$$

∴ State matrix

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 3 & 2 \\ -4 & -4 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 4 \\ 3 \end{bmatrix} u$$

$$y = [2 \quad 2]\begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

(ii) Check for the controllability and observability by Kalman's test,

Kalman's test for controllability:

$$[Q_c] = [B : AB : A^2B : .... : A^{n-1}B]$$

For given system,

$$[Q_c] = [B : AB]$$

where, $$[AB] = \begin{bmatrix} 3 & 2 \\ -4 & -4 \end{bmatrix}\begin{bmatrix} 4 \\ 3 \end{bmatrix} = \begin{bmatrix} 12+6 \\ -16-12 \end{bmatrix} = \begin{bmatrix} 18 \\ -28 \end{bmatrix}$$

∴ $$[Q_c] = \begin{bmatrix} 4 & 18 \\ 3 & -28 \end{bmatrix}$$

∵ $$|Q_c| \neq 0$$

Also, Rank of $[Q_c]$ = Rank of $[A]$

Hence, the given system is said to be controllable.

Kalman's test for observability:

$$[Q_0] = [C^T : A^TC^T : (A^T)^2C^T : .... : (A^T)^{n-1}\, C^T]$$

For given system,

$$[Q_0] = [C^T : A^TC^T]$$

where $$[A^TC^T] = \begin{bmatrix} 3 & -4 \\ 2 & -4 \end{bmatrix}\begin{bmatrix} 2 \\ 2 \end{bmatrix} = \begin{bmatrix} 6-8 \\ 4-8 \end{bmatrix} = \begin{bmatrix} -2 \\ -4 \end{bmatrix}$$

∴ $$[Q_0] = \begin{bmatrix} 2 & -2 \\ 2 & -4 \end{bmatrix}$$

∵ $|Q_0| \neq 0$ and Rank of $[Q_0]$ = Rank of $[A]$. The given system is observable.

Q.5 (d) Solution:

The open loop transfer function is

$$G(s)H(s) = \frac{K(s+3)(s+4)}{(s+1)(s+\alpha)}$$

For any point to lie on the root locus it must satisfy the angle condition as well as the magnitude condition.

i.e., $|G(s)H(s)| = 1$

and $\angle G(s)H(s) = \pm 180°$

For the point $(-2 + j3)$, the open loop transfer function becomes,

$$G(-2+j3)\,H(-2+j3) = \frac{K(-2+j3+3)(-2+j3+4)}{(-2+j3+1)(-2+j3+\alpha)}$$

$$= \frac{K(1+j3)(2+j3)}{(-1+j3)(\alpha-2+j3)}$$

and $$\angle G(-2+j3)\,H(-2+j3) = \tan^{-1}\frac{3}{1} + \tan^{-1}\frac{3}{2} - \tan^{-1}\left(\frac{3}{\alpha-2}\right) - 180° + \tan^{-1}\frac{3}{1}$$

$$= 71.56° + 71.56° - 180° + 56.31° - \tan^{-1}\left(\frac{3}{\alpha-2}\right)$$

$$= 19.429° - \tan^{-1}\left(\frac{3}{\alpha-2}\right)$$

$\because$ point $(-2 + j3)$ located on the root locus.

$\therefore$ $\angle G(-2+j3)\,H(-2+j3) = \pm 180°$

$$180° = 19.43° - \tan^{-1}\left(\frac{3}{\alpha-2}\right)$$

or $$\frac{3}{\alpha-2} = -\tan(160.57°)$$

$$\frac{3}{\alpha-2} = 0.353$$

or $\alpha = 10.50$

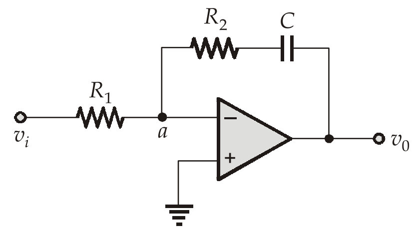
Q.5 (e) Solution:

The given transfer function is

$$G_c(s) = \frac{10s+4}{s} = 10 + \frac{4}{s} \quad \text{...(i)}$$

$$G_c(s) = K_p + \frac{K_I}{s}$$

Thus, the given controller is a PI controller. It can be realised using operational amplifier as



Using KCL at 'a' in s-domain, we get,

$$0 = \frac{0-V_i}{R_1} + \frac{0-V_0}{R_2 + \frac{1}{Cs}}$$

or $$\frac{V_0(s)}{V_i(s)} = -\frac{R_2}{R_1}\frac{\left(s+\frac{1}{R_2C}\right)}{s}$$

Here minus sign indicates inverting configuration

or, $$G_c(s) = \frac{R_2}{R_1} + \left(\frac{1}{R_1Cs}\right) \quad ...(ii)$$

On comparing equation (i) and (ii), we get,

$$\frac{R_2}{R_1} = 10$$

or $$R_2 = 10R_1 \quad ...(iii)$$

and $$\frac{1}{R_1C} = 4$$

or $$R_1C = \frac{1}{4} = 0.25 \quad ...(iv)$$

$\because$ $$C = 25\ \mu F \text{ (given)}$$

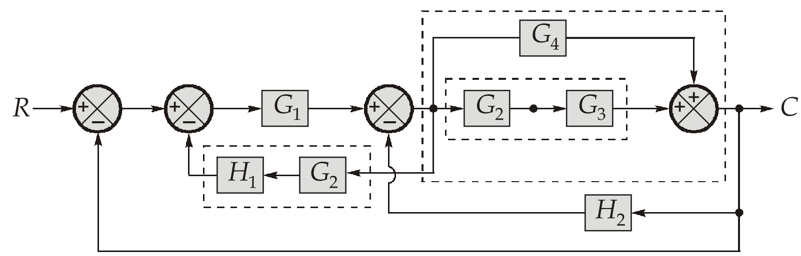
$\therefore$ $$R_1 = \frac{1}{4C} = \frac{0.25}{25\times10^{-6}} = 10\ k\Omega$$

and hence, from equation (iii)

$$R_2 = 100\ k\Omega$$

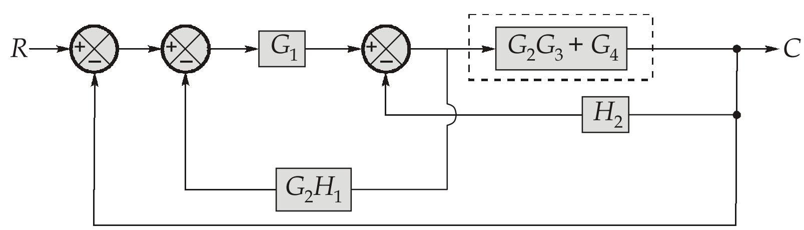
Q.6 (a) Solution:

(i) Moving the take off point ahead of G_2 in given block diagram, the modified diagram will be obtained as

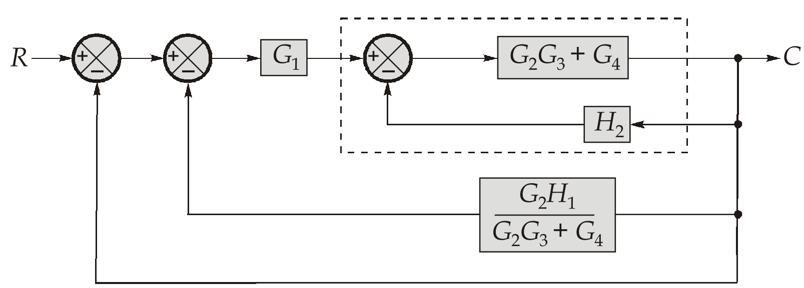


Here, blocks G_2 and G_3 are in cascade. They can be combined into a single block with a gain G_2G_3. Now blocks G_2G_3 and G_4 are in parallel. They can be combined into a single block with gain of $(G_2G_3 + G_4)$. Also, blocks G_2 and H_1 are in cascade. They can be combined into a single block with a gain of G_2H_1.

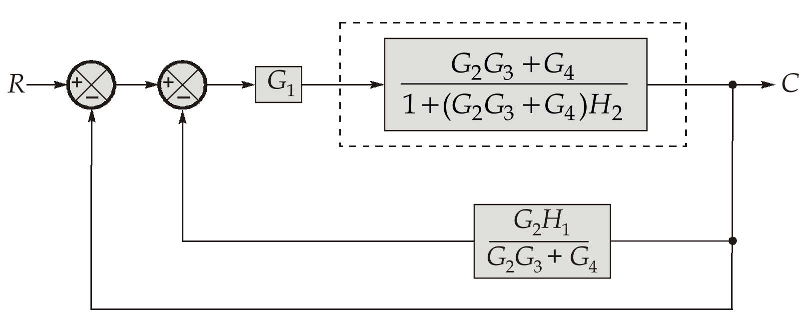
Thus, the resultant block diagram can be drawn as



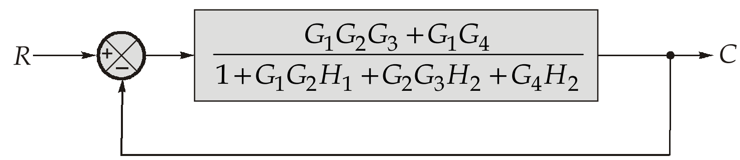
Now moving the take off point after the block $(G_2G_3 + G_4)$, the block diagram will be shown below as,



Simplifying the inner loop of above diagram the block diagram can be reduced as



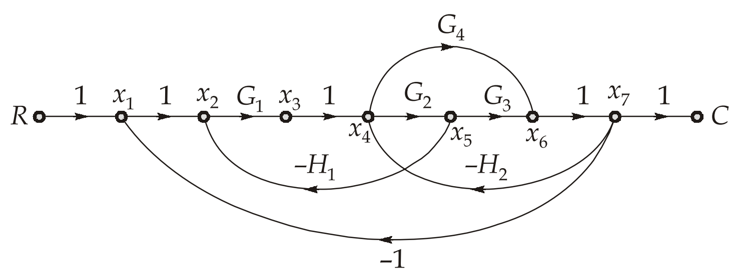
Combining the two blocks in cascade and then simplifying the inner loop, the block diagram can be modified as shown below as



Now, by simplifying the single loop, the resultant transfer function is obtained as

$$\frac{C}{R} = \frac{G_1G_2G_3+G_1G_4}{1+G_1G_2H_1+G_2G_3H_2+G_4H_2+G_1G_2G_3+G_1G_4}$$

(ii) The equivalent signal flow graph of the given block diagram can be drawn as shown below,



The forward paths and the corresponding gains are as follows:

$$P_1 \Rightarrow R - x_1 - x_2 - x_3 - x_4 - x_5 - x_6 - x_7 - C$$

$\therefore$ $$P_1 = G_1G_2G_3$$

and $$P_2 = R - x_1 - x_2 - x_3 - x_4 - x_6 - x_7 - C$$

$\therefore$ $$P_2 = G_1G_4$$

The individual loops and corresponding gains are as follows,

$$L_1 \Rightarrow -G_2G_3H_2$$
$$L_2 \Rightarrow -G_1G_2G_3$$
$$L_3 \Rightarrow -G_1G_2H_1$$
$$L_4 \Rightarrow -G_4H_2$$
$$L_5 \Rightarrow -G_1G_4$$

There are no loops which are non touching to each other.

Also, there is no loop which is non touching to the forward path of P_1 and P_2.

So, the determinant

$$\Delta_1 = \Delta_2 = 1$$

The determinant of signal flow graph can be given as

$$\Delta = 1 - (L_1 + L_2 + L_3 + L_4 + L_5)$$
$$= 1 + G_2G_3H_2 + G_4H_2 + G_1G_2H_1 + G_1G_2G_3 + G_1G_4$$

By using Mason's gain formula, the overall transfer function is

$$\frac{C}{R} = \frac{P_1\Delta_1 + P_2\Delta_2}{\Delta}$$

$$\frac{C}{R} = \frac{G_1G_2G_3 + G_1G_4}{1 + G_2G_3H_2 + G_4H_2 + G_1G_2H_1 + G_1G_2G_3 + G_1G_4}$$

Q.6 (b) Solution:

The closed loop transfer function of the given system is,

$$\frac{C(s)}{R(s)} = \frac{G(s)}{1+G(s)} = \frac{10}{s(s+2)+10} = \frac{10}{s^2+2s+10}$$

(i) To determine unit step response

$$C(s) = \frac{10}{s^2+2s+10} \times R(s)$$

$$C(s) = \frac{10}{s(s^2+2s+10)}$$

Using the partial fraction, the function $C(s)$ can be written

$$C(s) = \frac{A}{s} + \frac{Bs+C}{s^2+2s+10}$$

$$(A + B)s^2 + (2A + C)s + 10A = 10$$

Here, $10A = 10 \Rightarrow A = 1$

$\therefore$ $B = -1$

$\therefore$ $C = -2$

So, $$C(s) = \frac{1}{s} - \frac{s+2}{s^2+2s+10}$$

$$C(s) = \frac{1}{s} - \frac{(s+1)}{(s+1)^2+9} - \frac{1}{(s+1)^2+9}$$

Taking inverse Laplace transform, we get,

$$c(t) = \left[1 - e^{-t}\cos 3t - \frac{1}{3}e^{-t}\sin 3t\right]u(t)$$

(ii) The characteristic equation,

$$s^2 + 2s + 10 = 0$$

Comparing with characteristic equation of second order unity feedback system, we get,

$$\omega_n = \sqrt{10} = 3.16 \text{ rad/sec}$$

and $$2\xi\omega_n = 2$$

or $$\xi = \frac{2}{2\omega_n} = \frac{1}{3.16} = 0.32$$

Also, $$\omega_d = \omega_n\sqrt{1-\xi^2} = 3.16\sqrt{1-(0.32)^2} = 3 \text{ rad/sec}$$

(iii)

The peak time is the time at which maximum peak overshoot of the response appear.

$\therefore$ $$t_p = \frac{\pi}{\omega_d} = \frac{\pi}{3} = 1.047 \text{ sec}$$

% peak overshoot is

$$\%M_p = \frac{c(t_p)-1}{1}\times 100\% = e^{-\xi\omega_n t_p}\times 100$$

$$= e^{-(1)(1.047)}\times 100 \approx 35.1\%$$

(iv) Steady state error, for the input $(1 + 4t)\ u(t)$, is calculated as

Here, $$L[r(t)] = R(s) = \frac{1}{s} + \frac{4}{s^2} = \frac{s+4}{s^2}$$

Now, $$E(s) = \frac{R(s)}{1+G(s)} = \frac{1}{1+\frac{10}{s(s+2)}}\times\frac{s+4}{s^2} = \frac{s(s+4)(s+2)}{s^2(s^2+2s+10)}$$

$\therefore$ $$e_{ss} = \lim_{s\to 0} sE(s) = \lim_{s\to 0}\frac{s\times s(s+4)(s+2)}{s^2(s^2+2s+10)} = \frac{8}{10} = 0.8$$

$$e_{ss} = 0.8$$

(v) If poles are added at $\pm\sqrt{5}j$, thus $G(s)$ will have another denominator term of $(s^2 + 5)$

$\therefore$ $$G(s) = \frac{10}{s(s+2)(s^2+5)}$$

$\therefore$ characteristic equation,

$$1 + G(s) = 1+\frac{10}{s(s+2)(s^2+5)} = 0$$

$$\Rightarrow \quad s(s+2)(s^2+5)+10 = 0$$

$$s^4+2s^3+5s^2+10s+10 = 0$$

Using Routh's tabular form, we get,

s^4	1	5	10
s^3	2	10	0
s^2	$\frac{10-10}{2}$ (0)	5	
s^1			
s^0			

As zero has appeared in the first column of s^2 row, put $s = \frac{1}{z}$ in the characteristic equation, we get,

$$\left(\frac{1}{z}\right)^4 + 2\left(\frac{1}{z}\right)^3 + 5\left(\frac{1}{z}\right)^2 + \frac{10}{z} + 10 = 0$$

$$10z^4 + 10z^3 + 5z^2 + 2z + 1 = 0$$

Developing Routh's array, we get,

s^4	10	5	1
s^3	10	2	0
s^2	3	1	0
s^1	$-\frac{4}{3}$	0	
s^0	1		

As there are two sign changes in the first column of the Routh's array. Hence there are two roots lying in RHS of the s-plane. Hence, the closed loop system is unstable.

Q.6 (c) Solution:

To determine the unit step response:

- For unit step input, $\quad R(s) = \frac{1}{s}$

  So, $\quad C(s) = \frac{5(s+1)R(s)}{s^2+2s+5} = \frac{5(s+1)}{s(s^2+2s+5)}$

- By using the rules of partial fractions, we can write,

$$C(s) = \frac{5(s+1)}{s(s^2+2s+5)} = \frac{A}{s} + \frac{(Bs+C)}{s^2+2s+5}$$

$$(A + B)s^2 + (2A + C)s + 5A = 5s + 5$$

$$5A = 5 \Rightarrow A = 1$$

$$2A + C = 5 \Rightarrow C = 5 - 2A = 3$$

$$A + B = 0 \Rightarrow B = -A = -1$$

So, $$C(s) = \frac{1}{s} - \frac{s-3}{s^2+2s+5} = \frac{1}{s} - \frac{(s+1)-4}{(s+1)^2+4}$$

$$= \frac{1}{s} - \frac{(s+1)}{(s+1)^2+4} + \frac{4}{(s+1)^2+4}$$

- By applying inverse Laplace transform to $C(s)$, we get,

$$c(t) = \left[1 - e^{-t}\cos(2t) + 2e^{-t}\sin(2t)\right]u(t)$$

$$= \left[1 + 5e^{-t}\left(\frac{2}{5}\sin 2t - \frac{1}{5}\cos 2t\right)\right]u(t)$$

Unit step response, $$c(t) = [1 + 5e^{-t}\sin(2t - \phi)]\, u(t)$$

where, $$\sin\phi = \frac{1}{5} \text{ and } \cos\phi = \frac{2}{5}$$

To determine t_p and $\%M_p$:

- The given system has a zero. So, the standard formulas for t_p and $\%M_p$ cannot be used in this case.
- The determine "t_p", the following equation should be solved.

$$\left.\frac{dc(t)}{dt}\right|_{t=t_p} = 0$$

$$c(t) = [1 + 5e^{-t}\sin(2t - \phi)]\, u(t)$$

$$\frac{dc(t)}{dt} = -5e^{-t}\sin(2t - \phi) + 10e^{-t}\cos(2t - \phi)$$

$$= 25e^{-t}\left[\frac{2}{5}\cos(2t-\phi) - \frac{1}{5}\sin(2t-\phi)\right]$$

$$= 25e^{-t}\left[\cos\phi\cos(2t-\phi) - \sin\phi\sin(2t-\phi)\right]$$

$$= 25e^{-t}\cos(2t + \phi - \phi) = 25e^{-t}\cos(2t)$$

At $t = t_p$, $$\left.\frac{dc(t_p)}{dt}\right|_{t=t_p} = 0$$

$$25e^{-t_p}\cos(2t_p) = 0$$
$$\cos(2t_p) = 0$$
$$2t_p = (2n+1)\frac{\pi}{2}; \quad n = 0, 1, 2, ...$$
$$t_p = (2n+1)\frac{\pi}{4}; \quad n = 0, 1, 2, ...$$

At maximum peak overshoot,

$$t_p = \frac{\pi}{4}\text{ sec}$$

- The percentage maximum peak overshoot of the unit step response can be given by,

$$\%M_p = \frac{c(t_p)-1}{1}\times 100$$
$$c(t_p) = \left[1+5e^{-t}\sin(2t-\phi)\right]u(t)\Big|_{t=t_p=\frac{\pi}{4}}$$
$$= 1+5e^{-\pi/4}\sin\left(2\times\frac{\pi}{4}-\phi\right)$$
$$= 1+5e^{-\pi/4}\sin\left(\frac{\pi}{2}-\phi\right) = 1+5\cos\phi\, e^{-\pi/4}$$
$$\cos\phi = \frac{2}{5} \text{ and } \sin\phi = \frac{1}{5}$$

So,

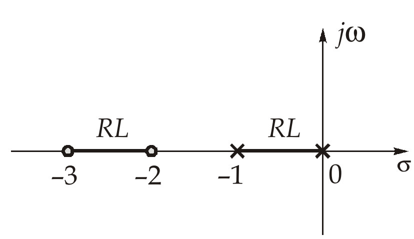
$$c(t_p) = 1+2e^{-\pi/4}$$
$$\%M_p = \frac{c(t_p)-1}{1}\times 100 = 2e^{-\pi/4}\times 100\% = 91.2\%$$

Q.7 (a) Solution:

The loop transfer function is,

$$G(s) = \frac{K(s+2)(s+3)}{s(s+1)}$$

By mere inspection $G(s)$ has two poles at $s = 0$ and $s = -1$ i.e., $p = 2$.
and two zeros at $s = -2$ and $s = -3$ i.e., $z = 2$.
This shows that there will be two root locus branches ($p = 2$) starting from two poles $s = 0$ and $s = -1$ and will terminate at the two zeros at $K = \infty$. The poles and zeros are plotted in figure.



$$\text{Number of asymptotes} = \text{Number of poles } (p) - \text{Number of zeros } (z)$$
$$= 2 - 2 = 0$$

Breakaway/breakin points

$$1 + G(s)H(s) = 0$$

$$1 + \frac{K(s+2)(s+3)}{s(s+1)} = 0$$

$$s^2 + s + K(s^2 + 5s + 6) = 0$$

$$K = \frac{-(s^2+s)}{s^2+5s+6}$$

$$\frac{dK}{ds} = -\frac{(s^2+5s+6)(2s+1)-(s^2+s)(2s+5)}{(s^2+5s+6)^2}$$

or $$s^2 + 3s + 1.5 = 0$$

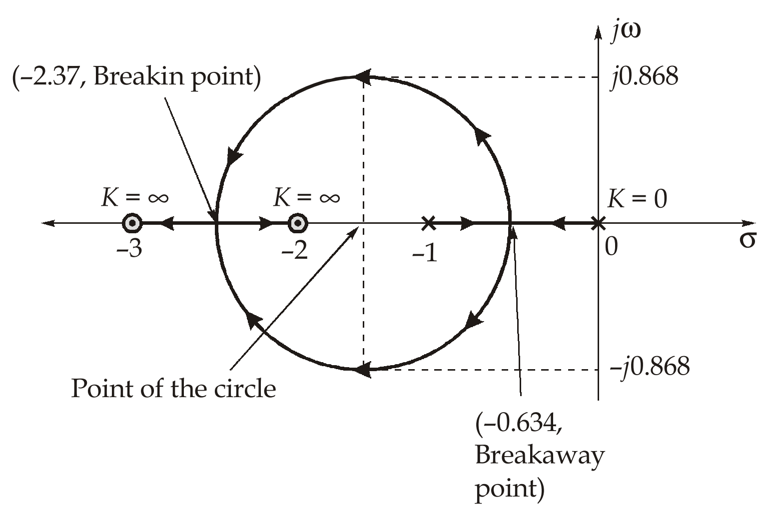
Solving, we get, $s = -2.37$ and -0.634

Therefore,

Breakaway point = –0.634 (as it is between two poles $s = 0$ and $s = -1$) and

Breakin point = –2.37 (between the zeros at $s = -2$ and $s = -3$).

The root loci will originate from $s = 0$ and $s = -1$ and move towards each other till $s = -0.634$; from where it will breakaway in a circular path at point $s = -2.37$. There will be a breakin point between $s = -2$ and $s = -3$ which are zeros. The root locus is shown in figure below.



Comments on how the value of K will make the system underdamped or overdamped

At the breakaway and breakin point value, $\xi = 1$, i.e., the system will be critically damped.

$$G(s)\Big|_{s=-0.634} = -1$$

or
$$\left.\frac{K(s+2)(s+3)}{s(s+1)}\right|_{s=-0.634} = -1$$

or
$$\frac{K(-0.634+2)(-0.634+3)}{-0.634(-0.634+1)} = -1$$

or
$$K = 0.072$$

and
$$G(s)\Big|_{s=-2.37} = -1$$

$$\left.\frac{K(s+2)(s+3)}{s(s+1)}\right|_{s=-2.37} = -1$$

or
$$\frac{K(-2.37+2)(-2.37+3)}{-2.37(-2.37+1)} = -1$$

or
$$K = 13.93$$

- The value of K at $s = -0.634$ is 0.072 and the value of damping ratio is 1, i.e., critically damped. The roots here are coincident. The value of K is zero at poles $s = 0$, i.e., origin and at $s = -1$.
- After the breakaway point, as K is increased, the root loci follow the circular path and till the breakin point $s = -2.37$, the value of damping ratio ξ is less than 1, i.e., the system is underdamped. The roots here are complex.
- The value of damping ratio ξ initially reduces from 1 at $s = 0.634$ to a low value at which the value of damping ratio is 0.89 and then starts increasing again and becomes equal to 1 (critically damped). The roots at breakin point are coincident.
- As K is increased further, i.e., between breakin point and point $s = -2$ and also between breakin point and $s = -3$, the damping ratio is greater than 1, i.e., overdamped case. The roots here are negative real.

Q.7 (b) Solution:

The characteristic equation for the given system is given by,

$$1 + G(s) = 0$$

$$1+\frac{K(s+4)}{s(s+1)(s+2)} = 0$$

or $s(s+1)(s+2) + K(s+4) = 0$

$\Rightarrow$ $s^3 + 3s^2 + (2+K)s + 4K = 0$

Using Routh's tabular form, we get,

s^3	1	$(2+K)$
s^2	3	$4K$
s^1	$\frac{6+3K-4K}{3}$	
s^0	$4K$	

(i) For system to be stable

$$4K > 0 \text{ or } K > 0$$

and $$\frac{6-K}{3} > 0$$

$\therefore$ The range of K is $0 < K < 6$.

(ii) The value of K which causes sustained oscillations is obtained by

$$\frac{6+3K-4K}{3} = 0$$

or $$6 - K = 0$$

or $$K = 6$$

$\therefore$ The frequency of oscillation is obtained by auxiliary equation,

$$A(s) = 3s^2 + 4K = 0$$

For $K = 6$; $$3s^2 + 24 = 0$$

or $$s^2 = -\frac{24}{3} = -8$$

or $$s = \pm j\sqrt{8} = \pm j2.828$$

$\therefore$ $$\omega = 2.828 \text{ rad/sec}$$

(iii)

When $K = 1$, the characteristic equation becomes,

$$s^3 + 3s^2 + 3s + 4 = 0$$

on solving the above equation, we get,

$$s = -2.44, -2.28 + 1.25j, -0.28 - j1.25$$

As the system has complex conjugate poles thus cannot have critically damped response.

Q.7 (c) Solution:

In the absence of time delay element, the transfer function is

$$G'(s) = \frac{10}{s(0.1s+1)}$$

For $s = j\omega$, the transfer function can be written as

$$G'(j\omega) = \frac{10}{j\omega(j0.1\omega+1)} \quad \text{...(i)}$$

The Nyquist plot for above function can be drawn as

For $\omega = 0$

$|G'(j\omega)| = \infty$

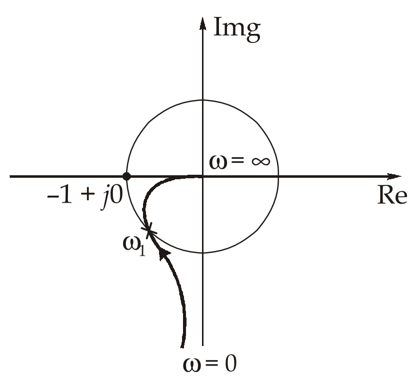
and $\angle\theta' = -90°$

For $\omega = \infty$

$|G(j\omega)| = 0$

and $\angle\theta' = -90° - \tan^{-1}\frac{\infty}{1} = -180°$

$\therefore$ The Nyquist plot can be drawn as



here, the gain cross over frequency ω_1 is determined as,

at $\omega = \omega_1$, $|G'(j\omega_1)| = 1$

$$|G'(j\omega_1)| = \left|\frac{10}{j\omega_1(j0.1\omega_1+1)}\right| = 1$$

or $$\frac{10}{\omega_1\sqrt{(0.1\omega_1)^2+1}} = 1$$

$\Rightarrow$ $$0.01\omega_1^4 + \omega_1^2 - 100 = 0$$

On solving above equation, we get,

$$\omega_1^2 = \frac{-1 \pm \sqrt{1^2 - 4 \times 0.01(-100)}}{2 \times 0.01} = (-0.5 \pm 1.118) \times 100$$

for positive sign,

$$\omega_1^2 = 61.8 \Rightarrow \omega_1 = 7.86 \text{ rad/sec} \quad \text{(ii)}$$

now, by incorporating time delay element $e^{-s\tau}$ the magnitude of $G'(j\omega)$ remain unaffected however the phase angle is modified as

$$\angle G'(j\omega_1) = -90° - \tan^{-1}(0.1\omega_1)$$
$$= -90° - \tan^{-1}(0.1 \times 7.86)$$
$$= -90° - \tan^{-1} 0.786$$
$$= -90° - 38.09° = -128.16°$$

$\therefore$
$$\text{PM} = 180° + \angle G'(j\omega_1)$$
$$= 180° - 128.16° = 51.84° \quad \text{...(iii)}$$

If the delay element get introduced, then the phase angle $\left(-\omega_1 T \times \frac{180}{\pi}\right)$ provided by the time delay element equals to –51.84° then, the limiting value of T for stability is determined as

$$\frac{-\omega_1 T \times 180°}{\pi} = -51.84° \quad \text{...(iv)}$$

$$\frac{-7.84 \times T \times 180°}{\pi} = -51.84°$$

or
$$T = 0.115 \text{ sec}$$

Q.8 (a) Solution:

The closed loop transfer function of the given system is

$$\frac{C(s)}{R(s)} = \frac{1}{s(1+s\tau)+K}$$

$\therefore$
$$C(s) = \frac{1}{s(1+s\tau)+K} \times R(s) = \frac{1 \times \frac{10}{s}}{s^2\tau + s + K}$$

The steady state value of the output

$$c(\infty) = \lim_{s \to 0} sC(s)$$

$$\therefore \quad 0.5 = \lim_{s \to 0} \frac{s \times \frac{10}{s} \times 1}{s^2\tau + s + K}$$

$$0.5 = \frac{10}{K}$$

or $$K = 20 \quad \text{...(i)}$$

For the given peak overshoot, the damping ratio can be calculated as

$$\%MPO = e^{-\pi\xi/\sqrt{1-\xi^2}} \times 100\%$$

$$0.05 = e^{-\pi\xi/\sqrt{1-\xi^2}}$$

or $$\frac{\pi\xi}{\sqrt{1-\xi^2}} = -\ln(0.05) = 2.996$$

or $$\xi^2 = 0.909(1 - \xi^2)$$

$\Rightarrow$ $$\xi^2 = \frac{0.909}{1.909} = 0.476$$

and $$\xi = 0.69 \quad \text{...(ii)}$$

and the peak time $$\tau_p = \frac{\pi}{\omega_d} = \frac{\pi}{\omega_n\sqrt{1-\xi^2}} = 2$$

$\Rightarrow$ $$\frac{2}{\pi} = \frac{1}{\omega_n\sqrt{1-0.69^2}}$$

or $$\omega_n = 2.17 \text{ rad/sec} \quad \text{...(iii)}$$

Comparing the given equation with standard second order characteristic equation, we get,

$$s^2 + \frac{1}{\tau}s + \frac{K}{\tau} = 0$$

Here, $$\omega_n^2 = \frac{K}{\tau} = (2.17)^2$$

or $$\frac{1}{\tau} = \frac{(2.17)^2}{K}$$

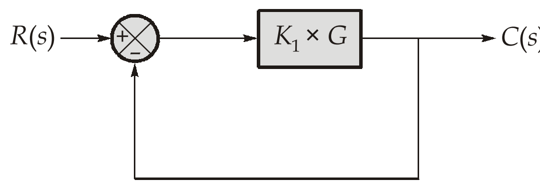
or $$\tau = \frac{K}{(2.17)^2} = \frac{20}{(2.17)^2} = 4.247$$

$\therefore$ $$K = 20$$

and $$\tau = 4.247$$

Q.8 (b) Solution:

From the given block diagram, the closed loop transfer function can be calculated as



where, $$G = \frac{\frac{1}{s(1+s)}}{1+\frac{K_2 s}{s(1+s)}} = \frac{1}{s(1+s)+K_2 s}$$

$\therefore$ $$\frac{C(s)}{R(s)} = \frac{K_1}{s^2+(K_2+1)s+K_1} \quad \text{...(i)}$$

Now we have, $$M_r = 1.41 = \frac{1}{2\xi\sqrt{1-\xi^2}}$$

or $$(2\xi)^2(1-\xi^2) = \left(\frac{1}{1.41}\right)^2 = 0.501$$

$$4\xi^2 - 4\xi^4 - 0.501 = 0$$

or $$4\xi^4 - 4\xi^2 + 0.501 = 0 \quad \text{...(ii)}$$

On solving above equation, we get,

$$\xi^2 = 0.85, 0.146$$

or $$\xi = 0.92, 0.382 \quad \text{...(iii)}$$

also $$\omega_r = \omega_n\sqrt{1-2\xi^2}$$

considering $\xi = 0.382$ and $\omega_r = 9$ rad/sec (given)

we get,

$$\omega_n = \frac{\omega_r}{\sqrt{1-2\xi^2}} = \frac{9}{\sqrt{1-2(0.382)^2}}$$

$$\omega_n = 10.696 \text{ rad/sec} \quad \text{...(iv)}$$

from equation (i) and (iv),

$$K_1 = \omega_n^2 = (10.696)^2 = 114.41$$

and $$(K_2+1) = 2\xi\omega_n = 2 \times 10.696 \times 0.382 = 8.172$$

$\Rightarrow$ $$K_2 = 7.172$$

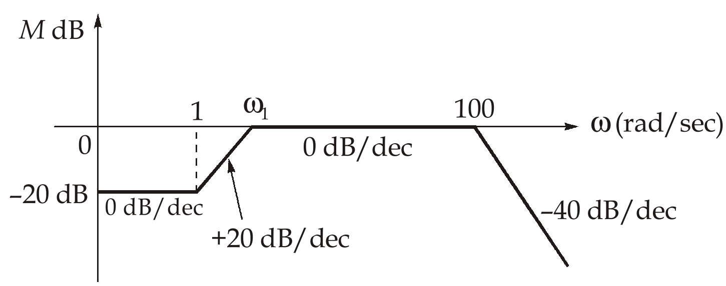
(ii)

The expression for closed loop transfer function is obtained from equation (i) and the value of K_1 and K_2 as

$$\frac{C(s)}{R(s)} = \frac{114.41}{s^2 + 8.172s + 114.41}$$

Q.8 (c) Solution:

(i) The given bode plot can be redrawn as



It can be seen that the initial slope is 0 dB/dec and intercept is –20 dB. This is only possible due to factor K. Since the intercept is minus, the value of K will be less than 1.

$$\therefore \quad 20\log K = -20$$

$$K = 0.1$$

Finding the value of ω_1:

From the slope between ω_1 and ω = 1 rad/sec

$$-\frac{0+20}{\log\omega - \log\omega_1} = 20 \text{ dB/dec}$$

$$-\frac{20}{\log\left(\frac{1}{\omega_1}\right)} = 20$$

or $$-\log\frac{1}{\omega_1} = 1$$

or $$\omega_1 = 10 \text{ rad/sec}$$

- Here, the slope of the line changes at ω = 1 rad/sec by +20 dB/dec thus, a zero is located at s = 1.
- At ω = 10 rad/sec the slope again changes to 0 dB/dec that is obtained by adding a pole in the system.

- Again at ω = 100 rad/sec the slope changes to –40 dB/dec which results in addition of two poles in the system.

∴ The resultant transfer function is

$$T(s) = \frac{K(1+s)}{\left(1+\frac{s}{10}\right)\left(1+\frac{s}{100}\right)^2} = \frac{0.1(1+s)\times 10\times 100^2}{(s+10)(s+100)^2}$$

$$T(s) = \frac{10^4(s+1)}{(s+10)(s+100)^2}$$

(ii) For unity feedback control system, the steady state error is given by,

$$e_{ss} = \lim_{s\to 0} sE(s) = \lim_{s\to 0}\frac{s\cdot R(s)}{1+G(s)} \quad \text{...(i)}$$

Here,

$$R(s) = L[r(t)]$$

$$= L[1+6t]\,u(t)$$

$$R(s) = \left[\frac{1}{s}+\frac{6}{s^2}\right] \quad \text{...(ii)}$$

∴ From equation (i) and (ii),

$$e_{ss} = \lim_{s\to 0}\frac{s\times\left[\frac{1}{s}+\frac{6}{s^2}\right]}{1+\frac{K(2s+1)}{s(5s+1)(s+1)^2}} = \lim_{s\to 0}\frac{s\times\frac{1}{s^2}(s+6)}{1+\frac{K(2s+1)}{s(5s+1)(s+1)^2}}$$

On solving the above equation, we get,

$$e_{ss} = \frac{6}{K} \quad \text{...(iii)}$$

Given that, $e_{ss} < 0.5$ for minimum value of K

∴ $$e_{ss} = 0.5 = \frac{6}{K}$$

or $$K = \frac{6}{0.5} = 12$$

∴ $$K_{min} = 12$$

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