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ELECTRONICS ENGINEERING
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By-KAMESH Sir

- Theory
- Explanation
- Derivation
- Example
- Shortcuts
- Previous Years Question With Solution

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Integrated Circuit

Circuit :-

Connection of active & Passive elements.

Active :-
- Transistors
- BJT
- MOSFET
- JFET etc.

Passive elements :- R, L, C etc.

Integrated Circuit :- In integrated circuit, all the active and passive elements are fabricated on the top of the substrate.

Substrate →
- Semiconductor
- Insulator

Integrated circuit	Discrete circuit
1. Small Size.	1. Large Size.
2. low power Consumption.	2. More power Consumption.
3. low cost. ↳ Because IC Fabrication is a batch process.	3. High Cost.
4. Non-repairable. (only replaced).	4. Can be repaired.

Classification of IC's :-

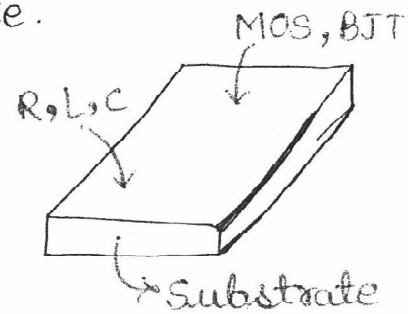
- On the basis of technology
  - → Monolithic IC's.
  - → Thin / Thick film IC's
  - → Hybrid IC's
- On the basis of level of Integration
  - → SSI
  - → MSI
  - → LSI
  - → VLSI
  - → ULSI
- Digital IC's / Analog IC's
  - → Bipolar IC's
  - → CMOS IC's
  - → BiCMOS IC's

∓ Monolithic IC's :

Mono – Single

Lithos – Stone

→ In monolithic IC's, all the active and passive elements are fabricated on the top of the single semiconductor substrate.

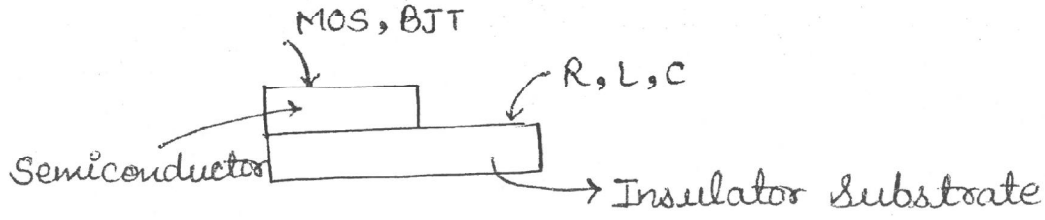


Disadvantages :-

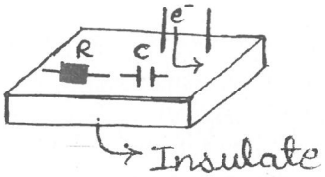
- Heavy value of R, L, C is avoided.
  (Restricted because they required or occupy large substrate area).

∓ Thin / Thick film IC's :- These IC's appear very similar in appearance. The only difference is the method by which the film is deposited.

→ For fabrication of active elements, semiconductor substrate is used & for fabrication of passive elements, Insulator substrate is used.

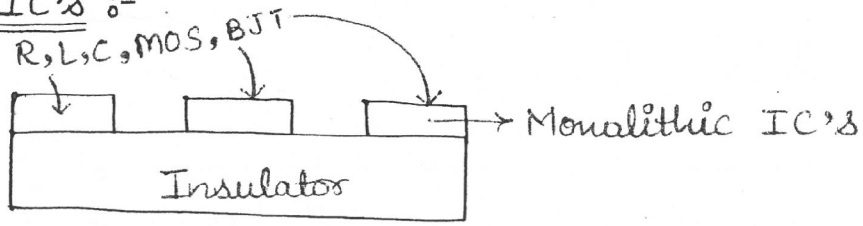


→ Heavy value of R, L, C is achieved compared to monolithic IC's.



Thin film	Thick film
1. The thin film is deposited by sputtering process. (or) Vapour Evaporation.	1. Thin film is deposited by Screen printing (or) Silk Screen printing.

Hybrid IC's :-



Level of Integration :-

1) SSI (Small Scale Integration): 1 - 10 transistors in per unit area of Substrate
2) MSI (Medium Scale Integration): $10 - 10^2$
3) LSI (Large " "): $10^2 - 10^4$
4) VLSI (Very large " "): $10^4 - 10^6$
5) ULSI (Ultra " " "): $> 10^6$

Packing density :- $P = \log_{10} Q$

$Q \rightarrow$ No. of transistors per unit area of the substrate.

SSI : $P < 1$

MSI : $1 < P < 2$

LSI : $2 < P < 4$

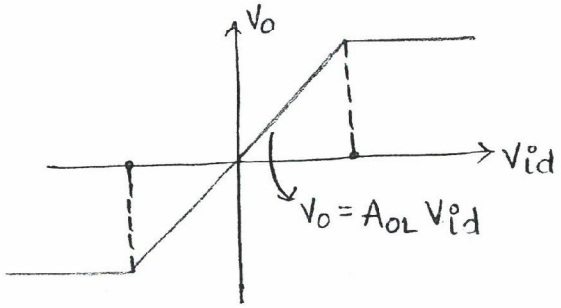
VLSI : $4 < P < 6$

ULSI : $P > 6$

Analog IC's :- (LINEAR IC)

I/P ⟶ Analog
O/P ⟶ Analog

Ex. : • IC - 555 timer
• OP-Amp



Digital IC's :- (Non-linear IC's)

I/P ⟶ Digital
O/P ⟶ Digital

Ex. : Flip-Flop

(BJT) # Bipolar IC's	(NMOS, PMOS) CMOS IC's
) Low packing Density.	① Packing density is high.
) High power Consumption	② Low power Consumption.
) High gain.	③ Low gain.
) High B.W.	④ Low B.W.
) High Speed	⑤ Low Speed.

Fick's law of diffusion →

1st law: $\boxed{J = -D \frac{\partial N}{\partial x}}$ — (1)

- $N \longrightarrow$ Concentration of atoms $[cm^{-3}]$
- $\frac{\partial N}{\partial x} \longrightarrow$ Concentration gradient of atoms (cm^{-4})
- $D \longrightarrow$ Diffusion Const. of atoms (or) Diffusivity of atoms (cm^2/sec)
- $^{\star}J \longrightarrow$ Atomic flux [No. of atoms crossing unit Cross-sectional area in per unit time]

2nd law :-

$$\nabla . J = \frac{-\partial N}{\partial t} \quad \text{— (2)}$$

$$\longrightarrow \frac{\partial J}{\partial x} = -\frac{\partial N}{\partial t}$$

$$\Rightarrow \frac{\partial}{\partial x}\left[-D \frac{\partial N}{\partial x}\right] = -\frac{\partial N}{\partial t}$$

$$D \frac{\partial^2 N}{\partial x^2} = \frac{\partial N}{\partial t}$$

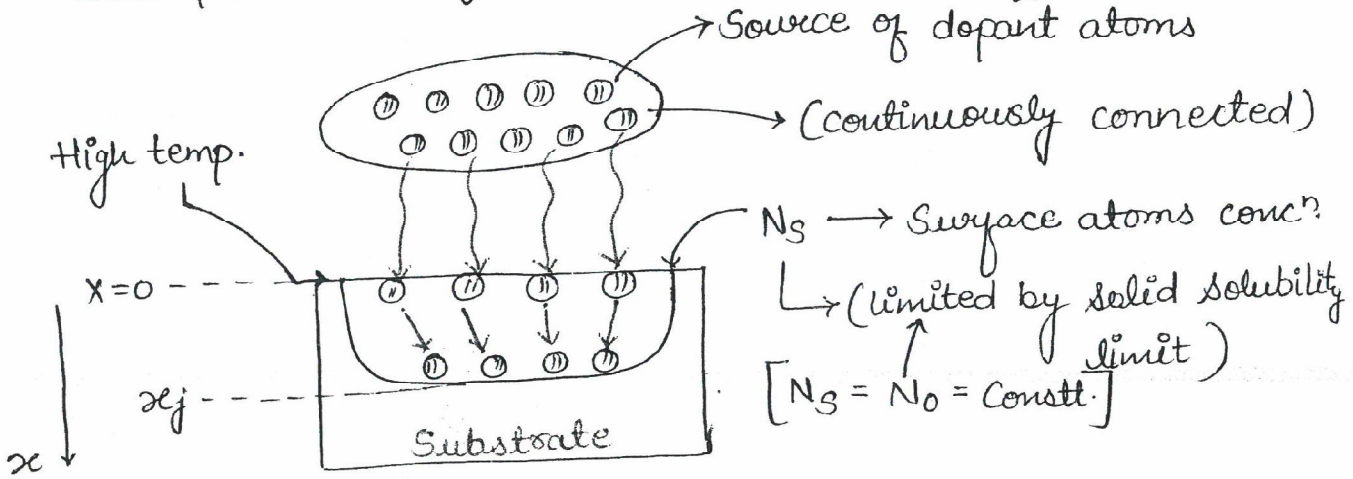
$$\Rightarrow \boxed{\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2}} \longrightarrow \text{Diffusion equation}$$

$\longrightarrow N(x,t) = ?$

⇒ Diffusion process of doping takes place in 2-steps —

1. Pre deposition (Infinite source diffusion)
2. drive-In (finite Source diffusion)

① Predeposition (Infinite / continuous source diffusion) :-



- x_j → Junction depth

→ Solid Solubility limit (N_0) :- The extend up to which a solid material can be dissolved in another solid material without precipitation.

$$D\frac{\partial^2 N}{\partial x^2} = \frac{\partial N}{\partial t} \longrightarrow N(x,t) = ?$$

Boundary Condition

→ ① $N(0,t) = N_0$

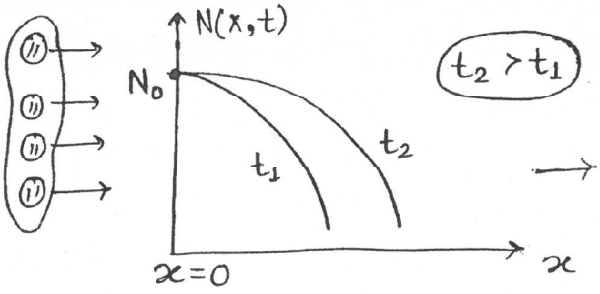
② $N(\infty,t) = 0$ → Deep doping is not possible.

③ $N(x,0) = 0$

After Solution ⇒

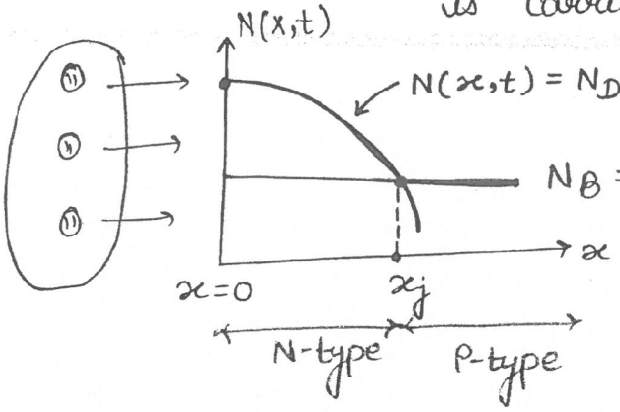
$$N(x,t) = N_0 \, erfc\left(\frac{x}{2\sqrt{Dt}}\right) cm^{-3}$$

erfc → complementary error function



→ complementary error fxⁿ profile

Ex. ⇒ Substrate is uniformly dopped P-type & doping of N-type is carried out →



⇒ At Junction :-

$$N(x,t) = N_B$$

$$N_0 \operatorname{erfc}\left(\frac{x_j}{2\sqrt{Dt}}\right) = N_B$$

$x_j = ?$

⇒ Doping parameters :-

1. Doping profile
2. Junction depth
3. Doping Dose

• Doping Dose :- [Q]

No. of dopant atoms / cm^2

$N(x,t) \longrightarrow$ atoms / cm^3

$$Q = \int_0^\infty N(x,t)\,dx \quad \text{atom}/cm^2$$

$$Q = \int_0^\infty N_0 \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) dx$$

$$\frac{x}{2\sqrt{Dt}} \longrightarrow v \text{ (let)}$$

$$dx = 2\sqrt{Dt}\, dv$$

limit :-

$x = 0 \Rightarrow v = 0$

$x = \infty \Rightarrow v = \infty$

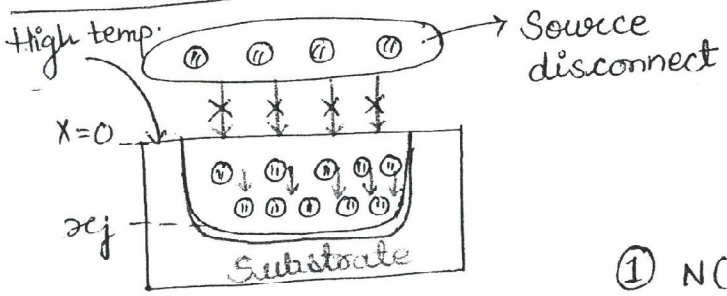
$$Q = \int_0^\infty N_0 \operatorname{erfc}(v)\, 2\sqrt{Dt}\, dv$$

$$Q = 2N_0\sqrt{Dt} \int_0^\infty \operatorname{erfc}(v)\, dv \longrightarrow \frac{1}{\sqrt{\pi}}$$

** (SN)

$$\boxed{Q = 2N_0\sqrt{\frac{Dt}{\pi}}} \text{ atoms/cm}^2$$

2) Drive - in :- (limited source diffusion)



$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2}$$

$N(x,t) = ?$

Boundary conditions

① $N(\infty, t) = 0$ (very deep doping is not possible)

② $\int_0^\infty N(x,t)\, dx = \text{Const.} = Q$

**

$$\boxed{N(x,t) = \frac{Q}{\sqrt{\pi Dt}}\, e^{-x^2/4Dt} \quad cm^{-3}}$$

Gaussian profile.

$$N_S = N(0,t) = \frac{Q}{\sqrt{\pi Dt}}$$

$t \uparrow$, $N_S \downarrow$