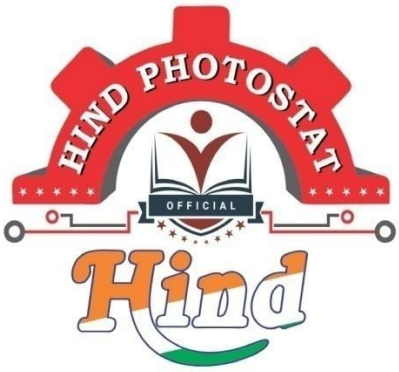



HindPhotostat


# Hind Photostat & Book Store

Best Quality Classroom Topper Hand Written Notes to Crack GATE, IES, PSU's & Other Government Competitive/ Entrance Exams

## MADE EASY
## ELECTRICAL ENGINEERING
### Analog Electronics
### By.A.Rajkumar Sir

- Theory
- Explanation
- Derivation
- Example
- Shortcuts
- Previous Years Question With Solution

Visit us:-www.hindphotostat.com

Courier Facility All Over India
(DTDC & INDIA POST)
Mob-9311989030

# HindPhotostat

GET IT ON Google Play

## EASY , , ACE , KREATRYX

**ESE , GATE, BEST** Y KW , / E E
D/E/D D W @

**1.** KE E /E / **2.** E /E /
D , E /E / **4.** / E /E /
/E D E /KE E /E / **6.** KD /

## ,GATE , TEST @

- –W / & D /
- **GATE**

➢ E **- ALL** E /E / E

➢ **ALL** sW / **YEAR** Y /KE W @

## W / /K K -

**EASY ,** **,ACE** **,KREATRYX ,GATE** /, **,GK**

, **YADAV, KD** D , &K E /KE , **–GRAW** , D ,W KE...K **S**

/ K @

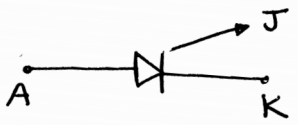
| | | | |
|---|---|---|---|
| F230, Lado Sarai<br>New Delhi-110030<br>Phone: 9311 989 030 | Shop No: 46<br>100 Futa M.G. Rd<br>Near Made Easy<br>Ghitorni, New Delhi-30<br>Phone:9711475393 | F518<br>Near Kali Maa Mandir<br>Lado Sarai<br>New Delhi-110030<br>Phone: 9560 163 471 | Shop No.7/8<br>Saidulajab Market<br>Neb Sarai More,<br>Saket, New Delhi-30 |

**Website: www.hindPhotostat.com**
**Contact Us: 9311 989 030**
**Courier Facility All Over India**
**(DTDC & INDIA POST)**

# -: Analog Electronics :-

## -: Chapter-1 Diode models :-

### Ideal model :-




Indication :

A → Anode (+)

K → cathode (−)

J → Junction

Arrow → unilateral device

↓

[impedance are different]

### conditions for ideal model of diode :-

$V_A - V_K > 0$ then D = ON — S.C. — $V_D = 0$, $I_D > 0$

$V_A - V_K < 0$ then D = OFF — O.C. — $V_D = V_B$, $I_D = 0$

$V_A - V_K = 0$ then D just ON — S.C. — $V_D = 0$, $I_D = 0$

$V_B$ = Battery voltage

### Testing method to check diode status :-

a. Short circuit Test (SC Test) [Failure when KVL violates in the ckt]

b. open circuit Test (OC Test) [Failure when KCL violates in the ckt]

### Procedure to check diode status using SC Test :-

Rule 1 :- Assume all the diodes to be S.C.

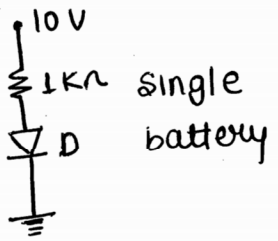
Rule 2 :- Indicate the current direction of each diode from A to K.

Rule 3 :- Check & calculate $I_D$ of each diode by using KVL & KCL

Status : $I_D > 0$ ; D = ON

$I_D < 0$ ; D = OFF

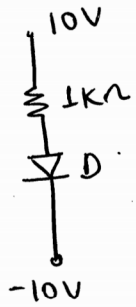
Example 1: Check the status of diode D in the given ckt



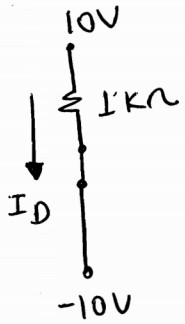

single battery


dual battery

Solution :-




$\Rightarrow$

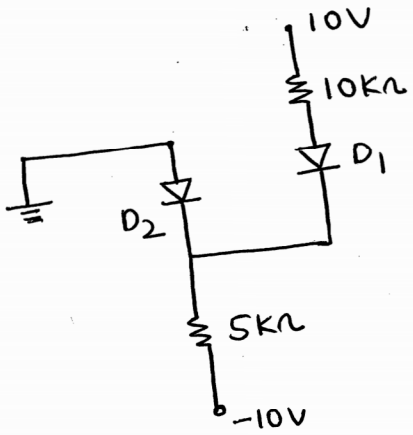



$$I_D = \frac{10-(-10)}{1K}$$

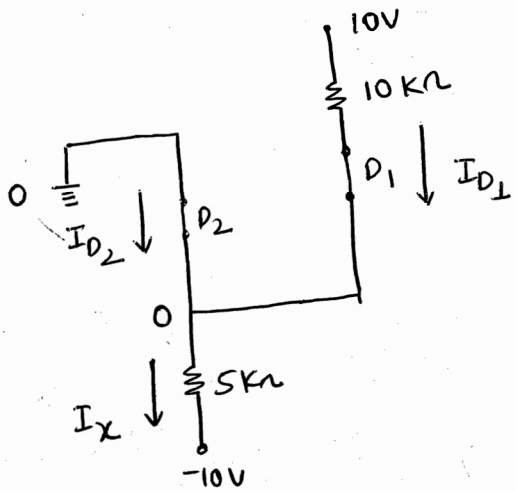
$$= 20mA > 0$$

$\hookrightarrow$ D ON

Example 2: check the status of $D_1$ & $D_2$ in the given ckt




Solution :-




$$I_{D_1} = \frac{10-(0)}{10K} = 1mA > 0$$

$\hookrightarrow$ $D_1$ ON

$$I_X = \frac{0-(-10)}{5K\Omega} = 2mA$$

KCL @ node 'a'

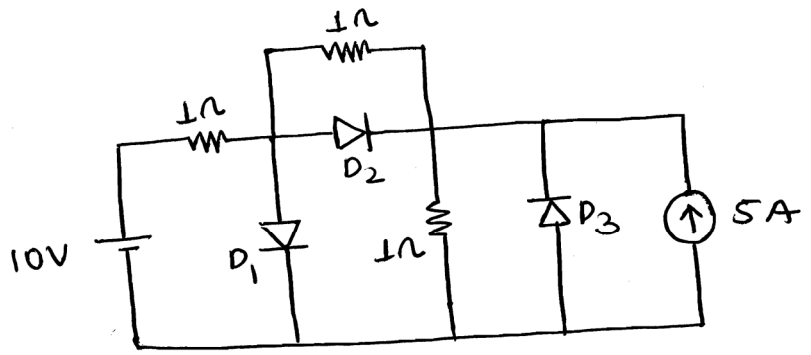
$$I_{D_1} + I_{D_2} = I_X$$

$$I_{D_2} = 2mA - 1mA$$

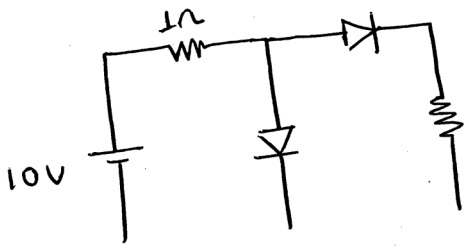
$$I_{D_2} = 1mA > 0$$

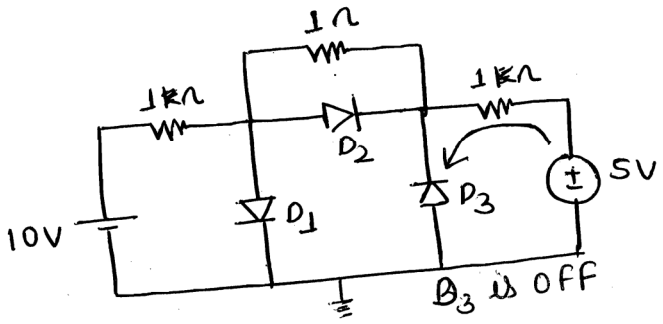
$\hookrightarrow$ $D_2$ ON

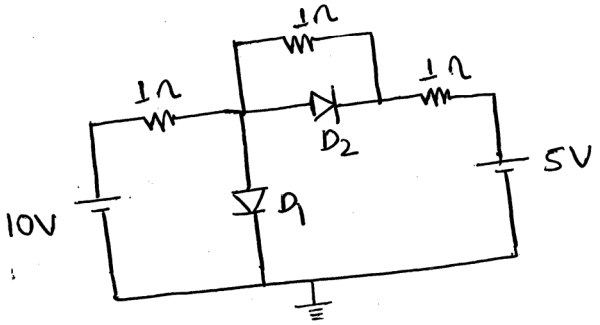
Q.N:- what are the states of the three ideal diodes of the circuit

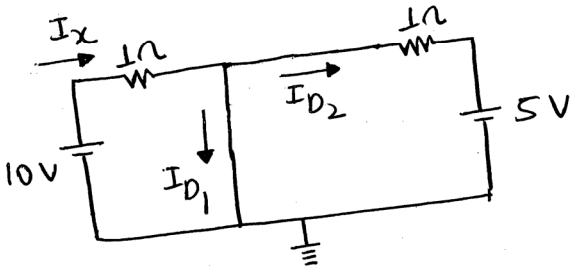



Solution:-




$I_x = \frac{10-0}{1} = 10A$ $\quad I_{D_2} = \frac{0-5}{1} = -5A < 0$ → $D_2$ is OFF

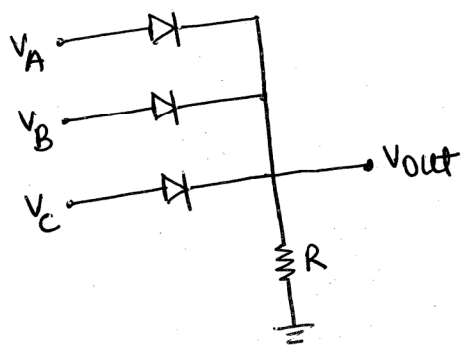
KCL at node a $\quad I_x = I_{D_1} + I_{D_2}$

$I_{D_1} = 10-(-5)$

$I_{D_1} = 15A > 0$

→ $D_1$ is ON

Conclusion:-




$V_A = 5V$, $V_B = 3V$, $V_C = 1V$

Failure of KVL in the short circuit test.

It violates KVL

$V_{out} = 5$ volt

Procedure to check diode status using open circuit test :-

Rule 1 : Assume all the diodes to be OFF

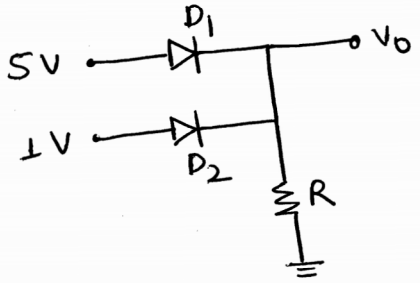
Rule 2 : Indicate $V_A$ & $V_K$ of each diodes

Rule 3 : Calculate $V_A - V_K$ difference of each diodes

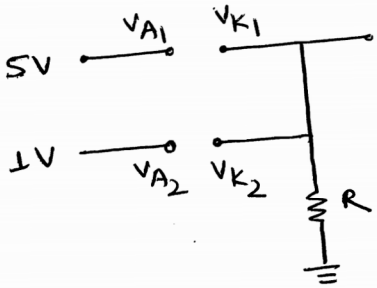
Status : $V_A - V_K > 0$ D = ON

$V_A - V_K < 0$ D = OFF

Example 1 :-




Solution :-




$V_{A_1} - V_{K_1} = 5 - 0$

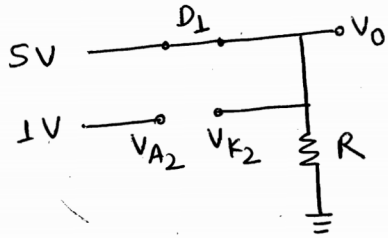
$= 5 > 0$

$V_{A_2} - V_{K_2} = 1 - 0$

$= 1 > 0$

Two diodes ON simultaneously then recheck condition

Select $D_1$ ON first because it is more FB



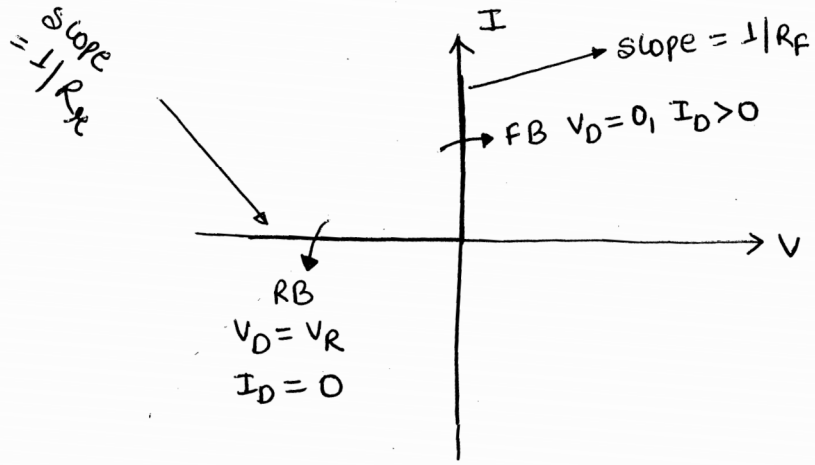

$V_{A_2} - V_{K_2} = 1 - 5$

$= -4 < 0$

$\rightarrow D_2$ become OFF

Highest voltage will be ON. first.

## V-I characteristic of ideal diode :-




Indication : $R_F$ = forward diode resistance

$R_R$ = Reverse diode resistance

In forward bias : $\text{slope} = \frac{1}{R_F} = \infty \Rightarrow \boxed{R_F = 0}$ ideal diode

In reverse bias : $\text{slope} = \frac{1}{R_R} = 0 \Rightarrow \boxed{R_R = \infty}$ ideal diode

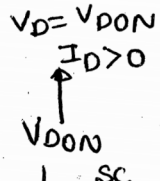
## CVD model :-

CVD means constant voltage drop model

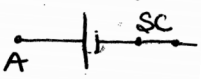
Practical diode will have cut in voltage $V_\gamma$.

$V_\gamma$ (si) ⟶ 0.5 V to 0.7 V

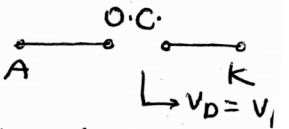
$V_D = V_\gamma$ then $V_D = V_{D,ON}$



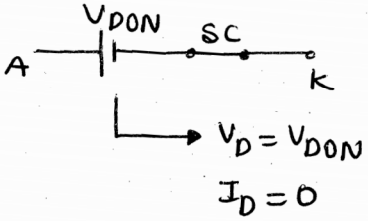

condition for CVD model :- $V_A - V_K > V_{D,ON}$ then D ON



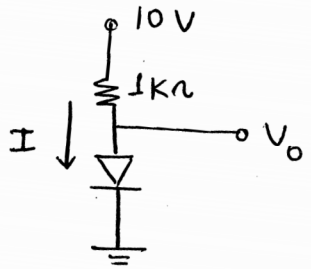

$V_A - V_K < V_{DON}$ then D = OFF



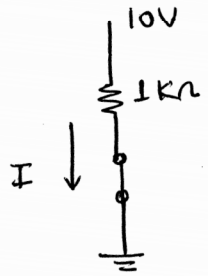

$V_A - V_K = V_{DON}$ then D just ON.



Ex 1 :- Check the status of diode and calculate $V_o$ and I using Ide
& CVD model.




Solution :- Ideal condition :- [SC Test]

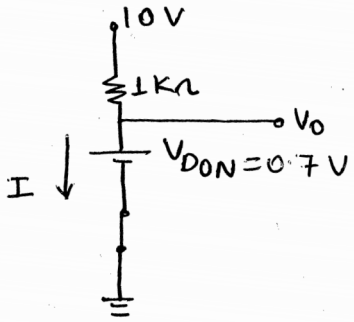



$$I = \frac{10-0}{1K}$$

$$= 10mA > 0 \text{ then } D \text{ ON}$$

$V = 0$, $I = 10mA$

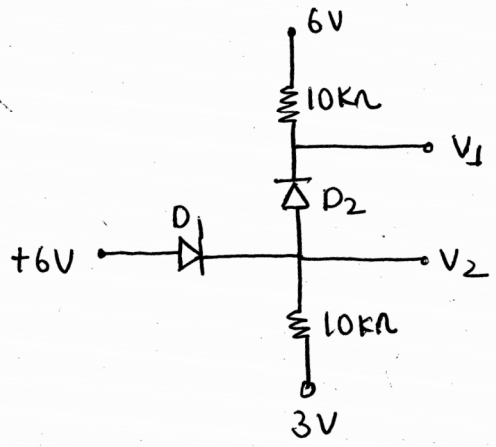
CVD condition :- [SC Test]



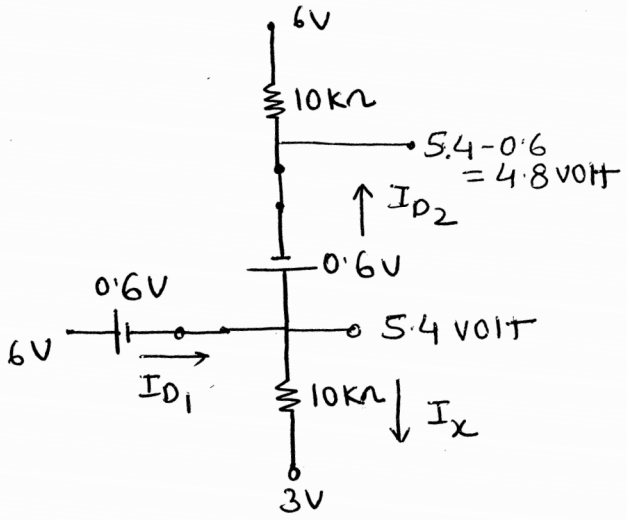

$$I = \frac{10-0.7}{1K} = 9.3mA > 0 \text{ then } D \text{ ON}$$

$V_o = 0.7$ volt, $I = 9.3mA$

Q.N:14 The voltage at $V_1$ & $V_2$ of the arrangement shown in figure will be respectively $V_\gamma = 0.6$ volt



Solution :-




$$I_x = \frac{5.4-3}{10K}$$

$$= 0.24\,mA$$

$$I_{D_2} = \frac{4.8-6}{10K}$$

$$= -0.12\,mA < 0$$

↳ $D_2$ is in OFF condition

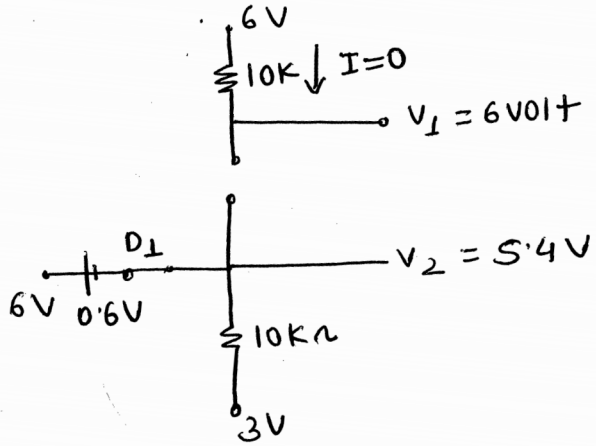
KCL @ 5.4V

$$I_{D_1} = I_{D_2} + I_x$$

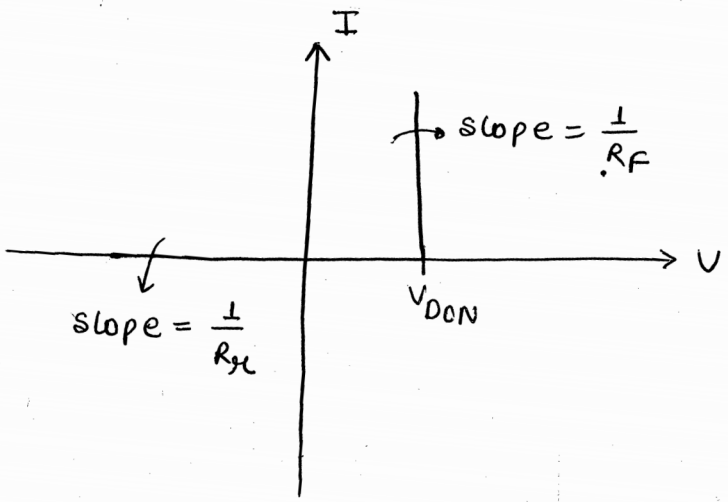
$$= -0.12 + 0.24$$

$$= 0.12\,mA > 0$$

↳ $D_1$ is in ON condition




## V-I characteristic of CVD model :-



In forward bias $\text{slope} = \frac{1}{R_f} = \infty$ $\boxed{R_f = 0}$

In reverse bias $\text{slope} = \frac{1}{R_r} = 0$ $\boxed{R_r = \infty}$

## PWL model :-

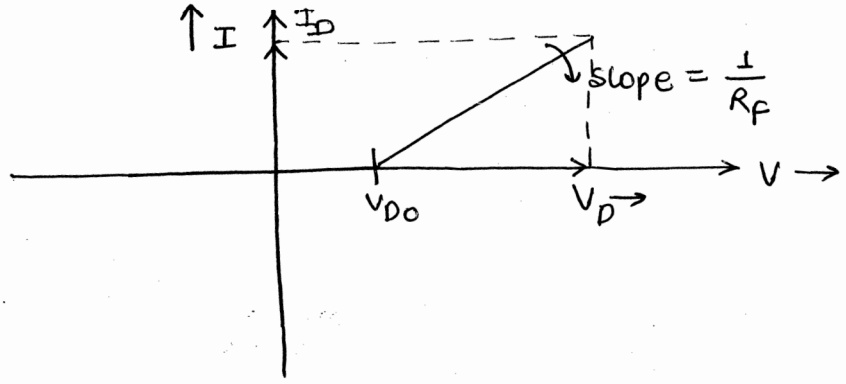
PWL means piece wise linear model

In PWL model : $V_{D0}$, $R_f$ will be given.

$V_{D0}$ : cut in voltage ($V_{D ON}$)

$R_f$ : forward resistance of diode

V-I characteristic of PWL model :-

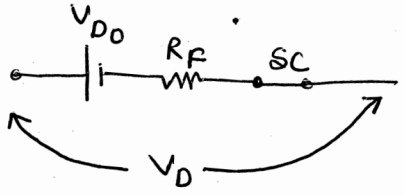



In forward bias $\text{slope} = \frac{1}{R_f} = \frac{I_D - 0}{V_D - V_{D0}}$

$$\boxed{R_f = \frac{V_D - V_{D0}}{I_D}}$$

conditions in PWL model :-

$V_A - V_K > V_{D0}$ D = ON




$V_A - V_K < V_{D0}$ D = OFF