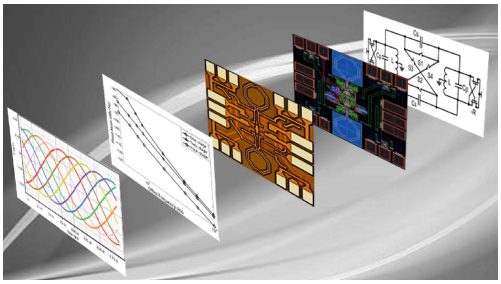
A text book on

Analog Circuits



Useful for IAS, IES, GATE, PSUs and other competitive examinations

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Dedicated to

My Wife

A. Smitha

who believes, in

The best teacher teaches from the heart,
…. not from the book….

PREFACE

I have great pleasure in writing the book of core subject of Electronics Engineering viz. **Analog Circuits.** A thorough understanding of the concepts developed in this book will prepare the reader for more advanced course on the subject. The entire syllabus of Analog circuits is presented in a simple and lucid style to make it comprehensible to an average student. This text book has been written to meet the requirements for the students of B.E./B.Tech., ECE, EEE, EIE.

In this book, I have tried to present the approach for competitive examinations like GATE, IES and IAS. While teaching various categories of students, I understood that, it becomes very easy for the students when things are explained by going through the fundamentals. So in the present book, I tried to explain most of the topics through the basics. The ***Questions with Solutions*** which already appeared in competitive examinations like GATE, IES are incorporated in each chapter.

First, I would like to thank **Mr. B. Singh** (Chief Managing Director, MADE EASY Group) for giving me the opportunity for writing the text book. His constructive suggestions and support helped me a lot.

I express my heartfelt regard and gratitude to my teacher Dr. Srinivas Rao from whom I have learnt the subject matter and which gave me inspiration to write this book.

I would also like to thank my H.O.D. Dr. Koteswara Rao and Principal Dr. Chinna Keshava Rao (CBIT), Mr. Sudarshan Reddy (Associate Prof. in CBIT) who always inspire me in discipline and hard work.

A special thanks to Mr. Sai Prasad who always, encourages me and gave me the first opportunity to teach for competitive exams.

I express my sincere gratitude to my favorite Sir, Mr. Prem R. Chadha, friends M.V. Kiran Kumar, Ramana Reddy, Krishna Kumar, Jagan, Krishna who always direct me in a right path.

Last but not the least, I also thank MADE EASY staff especially Vinod Kumar and Md. Asim who put their sincere efforts to develop this book in time.

Any comments and suggestions for the improvement of this book will be thankfully acknowledged and incorporated in the next edition.

A. Rajkumar

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CHAPTER 1

BJT BIASING & THERMAL STABILIZATION

About This Chapter

- Operating point and DC load line.
- AC load line.
- Stability factors S, S′ and S″.
- Various biasing circuits like fixed bias, collector to base bias and self bias.
- Compensation circuits.
- Thermal run-away and conditions to maintain thermal stability.

1 BJT Biasing & Thermal Stabilization

1.1 Operating Point and DC Load Line

- It is clear that the transistor functions most linearly when it is constrained to operate in its active region.
- To establish an operating point in this region it is necessary to provide appropriate direct potentials and currents, using external sources.
- Once an operating point Q is established as shown below:

ANALYSIS

Assume common emitter amplifier circuit

In DC analysis,

(i) ac should be grounded

(ii) $X_c \propto \frac{1}{f}$, as $f \to 0$, $X_c \to \infty$

$\therefore$ Capacitor is open.

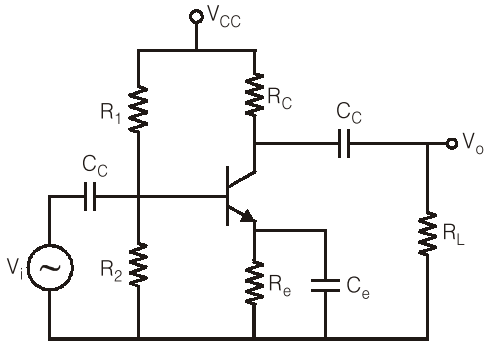


Figure 1.1 Common emitter amplifier

DC Equivalent Model

The output loop equation is given by

$$V_{CC} = I_C(R_C + R_e) + V_{CE}$$

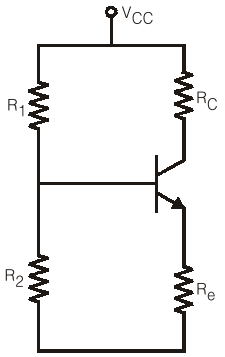
$$I_C = \frac{V_{CC}}{R_C + R_e} - \frac{V_{CE}}{R_C + R_e}$$

Above equation represents like a straight line y = mx + C

When $I_C = 0, \quad (V_{CE})_{max} = V_{CC}$

$$V_{CE} = 0, \quad (I_C)_{max} = \frac{V_{CC}}{R_C + R_e}$$

$$\text{Slope of DC load line} = -\frac{1}{R_C + R_e}$$



Output Characteristics of Common Emitter

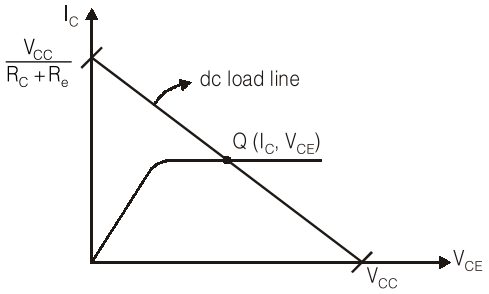


Fig. 1.2 DC load line and Q point

Q Point

"The intersection point between the dc load line and sample graph of I_C is called as operating point (or) Quiescent point".

DC Load Line

"The locus of all the Q points are concentrated on a line called as DC load line".

- When time varying excursions of the input signal (base current, for example) is applied to common emitter amplifier, should cause an output signal (collector voltage or collector current) of the same wave form.
- If the output signal is not a faithful reproduction of the input signal, for example, if it is clipped on one side. The operating point is unsatisfactory and should be relocated on the collector characteristics.
- The question now naturally arises as, how to choose the operating point.
- Note that even if we are free to choose R_c, R_L, R_b and V_{CC}, we may not operate the transistor every where in the active region, because the various transistor ratings limit the range of useful operation.
- These ratings are

  (i) $(V_{CE})_{max}$ **(ii)** $(I_C)_{max}$ **(iii)** $P_{c\,max}$

Capacitive Coupling

- The capacitor C_{b1} is to couple the input signal to the transistor, as indicated in the Figure (1.3).
- In this diagram, one end of V_i is at ground potential, and the collector supply V_{CC} also provides the biasing base current I_B.
- Under quiescent conditions (no input signal), C_{b1} (called a blocking capacitor) acts as an open circuit because the reactance of a capacitor is infinite at zero frequency (dc).

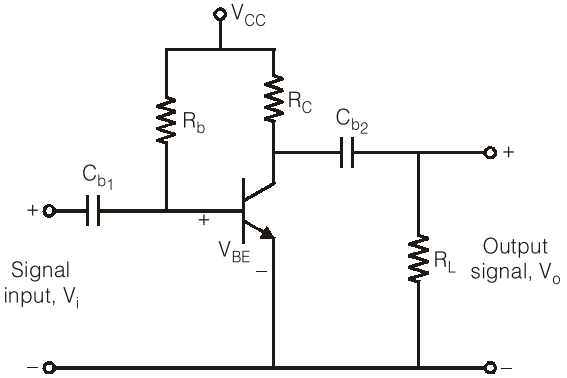


Figure 1.3 Fixed bias circuit

- The capacitances C_{b1} and C_{b2} are chosen large enough so that, at the lowest frequency of excitation their reactances are small enough so that they can be considered to be short circuits.
- These coupling capacitors block dc voltages but freely pass signal voltages.

  For example, the quiescent collector voltage does not appear at the output, but V_o is an amplified replica of the input signal V_i.
- The ac output signal voltage may be applied to the input of another amplifier with out affecting its bias, because of the blocking capacitor C_{b2}.

DC and AC Load Lines

- We noted that under dc conditions C_{b2} acts as an open circuit. Hence the quiescent collector current and voltage are obtained by drawing a static (dc) load line.
- If $R_L = \infty$ and if the input signal (base current) is large and symmetrical, we must locate the operating point Q_1 at the centre of the DC load line. In this way the collector voltage and current may vary approximately symmetrically around the quiescent values V_C and I_C respectively.

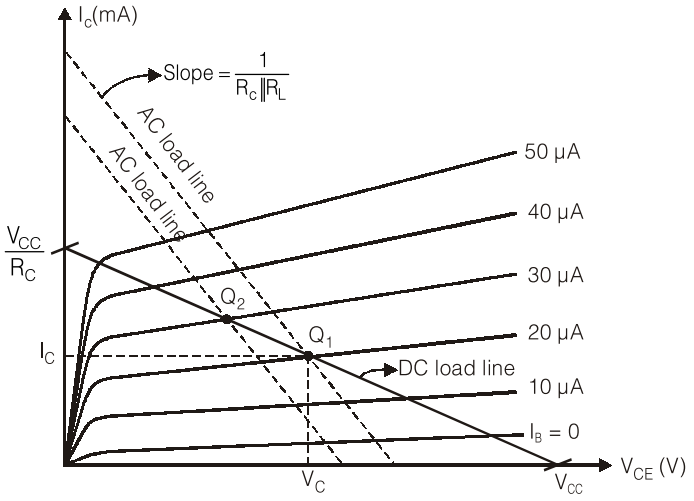
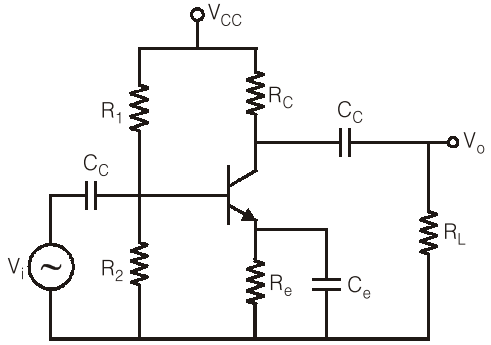


Figure 1.4 DC and AC load line

- If $R_L \neq \infty$, however, a dynamic (ac) load line must be drawn.
- Since, we have assumed that, at the signal frequency, C_{b2} acts as a short circuit, the effective load R_L' at the collector is R_C in parallel with R_L.

AC Load Line Analysis

Assume CE amplifier circuit:



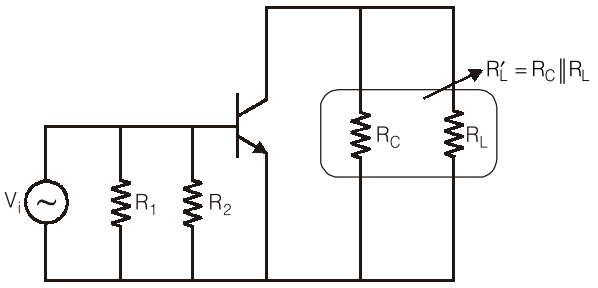
AC Analysis

(i) DC should be grounded.

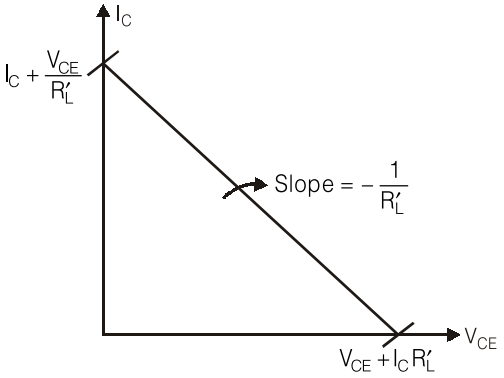
(ii) $X_C \propto \frac{1}{f}$, as $f \to \infty \therefore X_c \to 0$

i.e. capacitor acts as short circuit.

AC Equivalent Model



AC Load Line



$$\text{Slope of ac load line is } -\frac{1}{R'_L} = -\frac{1}{R_C \| R_L}$$

- We observe that the input signal may swing a maximum of approximately 20 μA around Q_1 because, if the base current decreases by more than 20 μA, the transistor is driven off.
- If a larger input swing is available, then in order to avoid cut-off during a part of the cycle. The quiescent point must be located at a higher current.
- Suppose we locate Q_2 on the dc load line such that a line with a slope corresponding to the ac resistance R'_L and drawn through Q_2 gives as large as output as possible with out too much distortion.
- The choice of Q_2 allows an input peak current swing of about 30 μA.

1.2 Temperature Dependence on Transistor Parameters

The sources of instability of I_C are essentially three:

(i) Reverse saturation current I_{CO}

(ii) Base-emitter voltage V_{BE}

(iii) Current gain β

- **I_{CO} Versus Temperature**

  "I_{CO} increases by 7%/°C rise in temperature".

  (or)

  "I_{CO} doubles for every 10°C rise in temperature".

  i.e. as temperature increases, I_{CO} also increases.

- **V_{BE} Versus Temperature**

  "The base to emitter voltage V_{BE}, which decreases at the rate of 2.5 mV/°C for both Ge and Si transistors."

  $$\frac{dV_{BE}}{dT} = -2.5 \text{ mV/°C}$$

  i.e. as temperature increases, V_{BE} decreases.

- **β Versus Temperature**

  (a) β increases with temperature

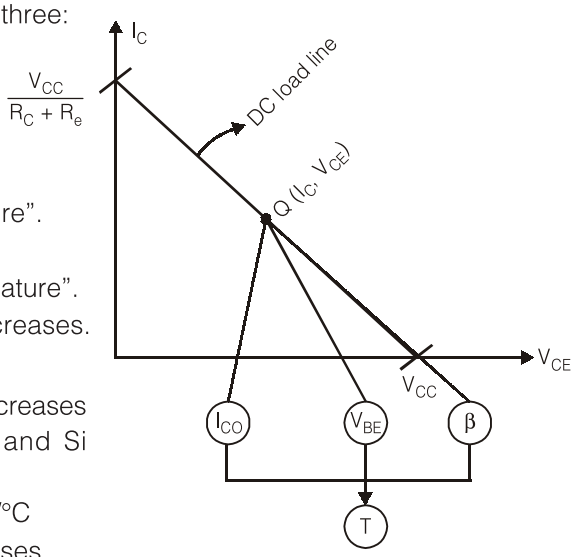


Figure 1.5 DC load line and Q point

(b) Replacement of Transistor

- We see that the spacing of the output characteristics will increase or decrease as β increases or decreases.
- Though transistors are identified by a type number, but even for a given type, the characteristics differ from piece to piece.
- β is the ratio of collector current I_C and base current I_b. As for the same base current, the collector current of the transistor will vary from replacement of the device.
- Generally β is greater for the replacement of transistor.

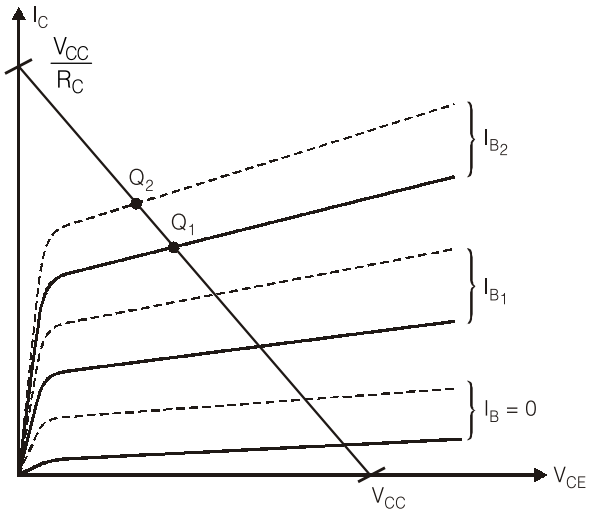


Figure 1.6 Common emitter characteristics

1.3 Stability Factor

"It is a measure of variation in the operating point with respect to the temperature is called as stability factor".

I_C is a function of I_{CO}, V_{BE} and β. It is convenient to introduce the three partial derivatives of I_C with respect to these variables. These derivatives are called the stability factors S, S′ and S″.

$$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}}$$

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}}$$

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}}$$

Expression for Stability Factor

$$I_C = \beta I_b + (1+\beta) I_{CO} \quad \text{d.w.r.t } I_C$$

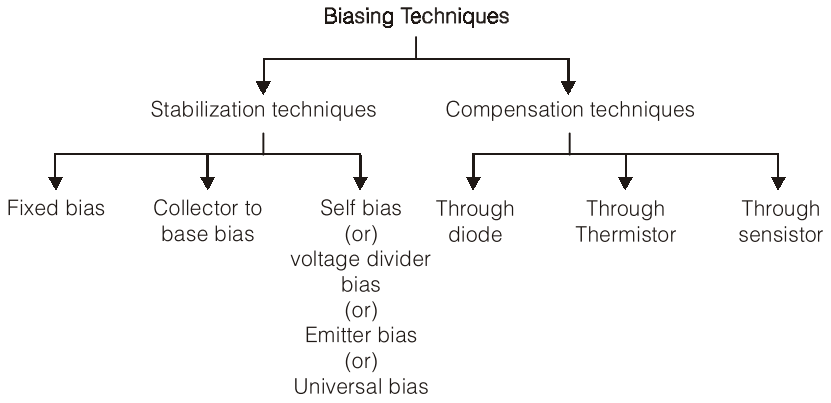
$$1 = \beta \frac{\partial I_b}{\partial I_c} + (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\boxed{S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\dfrac{\partial I_b}{\partial I_c}}}$$

Conclusion:

- Ideally the stability factor should be zero.
- Practically stability factor should be very very less.

1.4 Biasing Techniques



1.5 Fixed Bias Circuit

- From fixed bias circuit Figure (1.7) there is one resistance R_b connected between base and V_{cc}, through which the base current I_B flows.
- To make the Q point stable, base current I_B should be constant.

The input loop is

$$V_{CC} = I_B R_b + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_b}$$

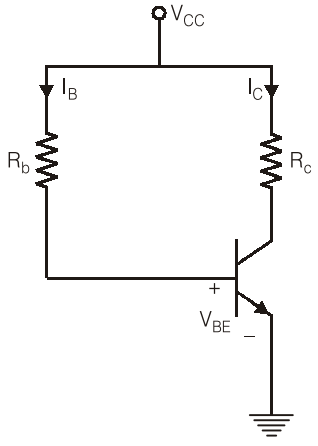


Figure 1.7 Fixed bias circuit

The voltage V_{BE} across the forward biased emitter junction is approximately 0.2 V for a germanium transistor and 0.7 V for a silicon transistor in the active region.

Since V_{CC} is usually much larger than V_{BE}, we have

$$I_B \approx \frac{V_{CC}}{R_b}$$

The current I_B is constant, and the network of Fig. (1.7) is called the fixed bias circuit.

Disadvantages of fixed bias circuit

(i) $I_C = \beta I_B$

β: Varies with temperature and transistor replacement

I_B: Constant

$\therefore$ If I_B is constant also, β may vary with respect to temperature.

(ii) Stability factor $S = \dfrac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_c}}$

In fixed bias $I_B \approx \dfrac{V_{CC}}{R_b}$

d.w.r.t. I_C $\dfrac{\partial I_B}{\partial I_C} = 0$

$\therefore$ $S = 1 + \beta$

Assume $\beta = 100$

$\therefore$ $S = 1 + 100 = 101$

For Q point stability, stability factor S should be very less.

1.6 Collector to Base Bias

- collector base bias circuit, shown in Figure (1.8) is an improvement over the fixed bias method.
- We know that the biasing resistance R_b is connected between the collector and the base of the transistor.
- Let us assume the base current as I_B and the collector current as I_C. So I_B flows through R_b and $(I_C + I_B)$ flows through collector resistance R_C.
- If there is a change in β (due to characteristic variation between transistors), or if there is any increase of ambient temperature, collector current I_C tends to increase.
- Finally, voltage drop $I_C R_C$ increases. Since supply voltage V_{CC} is constant, therefore V_{CE} decreases.
- This reduced V_{CE} results in reduced current I_B through R_b.

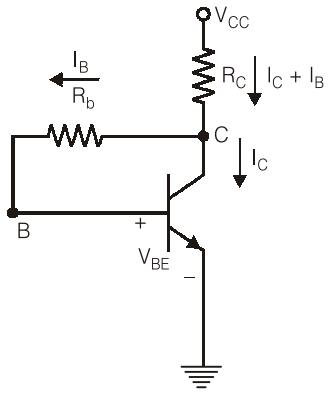


Fig. 1.8 Collector to base bias

ANALYSIS

Stabilization Concept

The input loop is given as

$$V_{CC} = (I_B + I_C) R_C + I_B R_b + V_{BE}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_b + R_C} \quad \text{...(i)}$$

The output loop is given as

$$V_{CC} = I_C R_C + V_{CE} + I_b R_C$$

$$V_{CC} - I_C R_C = V_{CE} + I_b R_C \quad \text{...(ii)}$$

From equation (i) and (ii)

$$I_B \text{ (Input parameter)} = \frac{V_{CE} + I_B R_C - V_{BE}}{R_b + R_C} \quad (\text{Output parameter})$$

- Since now the base current I_B is reduced, the collector current is reduced. Thus, we find that the collector-to-base biasing helps to partly compensate the changes which occurred originally due to change in temperature or change in β.

Stability Factor S for Collector to Base Bias

We can determine the stability factors S for the circuit, by applying KVL to the input loop

$$V_{CC} = (I_B + I_C) R_C + I_B R_b + V_{BE}$$

d.w.r.t I_C

$$0 = R_C + \frac{\partial I_B}{\partial I_C}(R_b + R_c) + 0$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_b + R_c}$$

$$S = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_c}}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\dfrac{R_c}{R_b + R_c}}}$$

It is an advantage compared to fixed bias circuit.

$\therefore$ This value is smaller than $(1 + \beta)$, which was the stability factor S for fixed bias circuit. Thus there is an improvement of stability in the collector-to base bias circuit.

Stabilization Against Change in β

$$I_C = (1 + \beta) I_{CO} + \beta I_B \quad \text{as} \quad \beta >> 1$$

$$I_C = \beta I_{CO} + \beta I_B \quad ; \quad I_B = \frac{I_C}{\beta} - I_{CO}$$

$$V_{CC} = (I_B + I_C)R_c + I_B R_b + V_{BE} \quad ; I_C = \beta\frac{(V_{CC} - V_{BE} + (R_b + R_C)I_{CO})}{\beta R_C + R_b}$$

$\beta R_c >> R_b$

$$I_C = \frac{V_{cc} - V_{BE} + (R_b + R_c)I_{co}}{R_c}$$

The collector current has become independent of β and hence stabilized against change in β.

Drawback

Always, it is not possible to maintain the above condition (i.e. $\beta R_C >> R_b$). For example, if the load resistance R_C is very small (as in a transformer coupled load), βR_C is in fact less than R_b. Thus for low values of R_C, the collector to base bias offers no improvement in stabilization as compared to fixed bias circuit.

1.7 Voltage Divider Bias or Self Bias

- In voltage divider bias circuit, the biasing is provided by three resistors (R_1, R_2 and R_e).
- The resistors R_1 and R_2 act as a potential divider giving a fixed voltage to the base.
- If the collector current I_C tends to increase (due to reasons like change in temperature or change in β). The emitter current I_E also increases and the voltage drop across R_e increases. The voltage difference between base and emitter will reduce and hence base current I_B will reduce. In turn, I_C will reduce, trying to partly compensate for the original change. This type of biasing improves stability.
- In order to prevent the instability of gain due to R_e, it is advantages to bypass R_e by a large value capacitor C_e. This gives the advantage of self bias, while maintaining the gain equal to that of a C.E. amplifier without R_e.

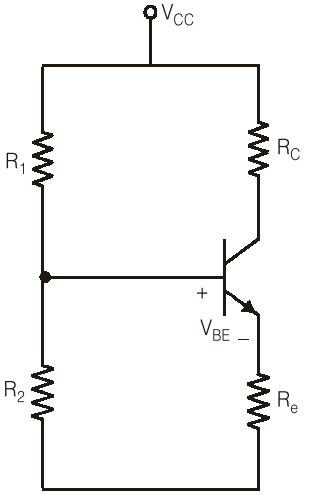


Figure 1.9 Voltage divider bias

Stability Factor S

To find the stability factor S, we first replace the voltage divider network R_1, R_2 by its Thevenins equivalent, as shown

Applying KVL around the base circuit loop

$$V = I_B R_b + V_{BE} + (I_B + I_C) R_e$$

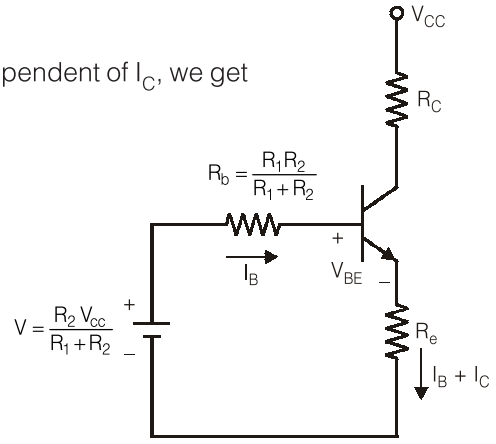
Differentiating w.r.t I_C and considering V_{BE} to be independent of I_C, we get

$$0 = \frac{\partial I_B}{\partial I_C} \cdot R_b + \frac{\partial I_B}{\partial I_C} R_e + R_e$$

$$\frac{\partial I_B}{\partial I_C}(R_b + R_e) = -R_e$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_e}{R_b + R_e}$$

$$S = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}} = \frac{1+\beta}{1+\beta\dfrac{R_e}{R_b + R_e}}$$



From the above equation, we have

(i) If $\dfrac{R_b}{R_e} << 1$, then Stability factor (S) = $(1+\beta)\cdot\dfrac{1}{(1+\beta)} = 1$

(ii) In the designing of the biasing circuit, R_b value should be less. i.e. R_1 and R_2 will be taken less values. If suppose R_1 is very less in the circuit, then the life time of the battery will be less. So, we take $R_1 > R_2$ to overcome this disadvantage.

(iii) R_e should be large. If it is consider, the negative feedback in the circuit increases which reduces the voltage gain. So keep a shunt capacitor parallel to R_e.

Stability Factor S′

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

From the input loop, $V = I_B R_b + V_{BE} + (I_B + I_C) R_e$

Where $I_B = \frac{I_C}{\beta} - \frac{(1+\beta)}{\beta} I_{CO}$

$$V_{BE} = V + (R_b + R_e)\frac{(1+\beta)}{\beta} I_{CO} - \frac{R_b + (1+\beta)R_e}{\beta} I_C$$

d.w.r.t V_{BE}

$$1 = 0 + 0 - \frac{R_b + (1+\beta)R_e}{\beta}\frac{\partial I_C}{\partial V_{BE}}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_b + (1+\beta) R_e}$$

$$\text{Stability factor (S)} = \frac{1+\beta}{1+\beta\frac{R_e}{R_b + R_e}} = \frac{(1+\beta)(R_b + R_e)}{R_b + (1+\beta) R_e}$$

$$\frac{S}{(1+\beta)(R_b + R_e)} = \frac{1}{R_b + (1+\beta) R_e}$$

$$S' = -\beta \frac{S}{(1+\beta)(R_b + R_e)}$$

$$\boxed{S' = \frac{S}{R_b + R_e}}$$

The lower the value of S, the lower is the value of S′,

Stability Factor S″

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{co} \text{ and } V_{BE} \text{ constant}}$$

$$V_{BE} = V + (R_b + R_e)\frac{(1+\beta)}{\beta} I_{CO} - \frac{R_b + R_e(1+\beta)}{\beta} I_C = V + V_1 - \frac{R_b + R_e(1+\beta)}{\beta} \cdot I_C$$

Where $V_1 = (R_b + R_e) I_{co} \cdot \frac{\beta + 1}{\beta}$; $I_C = \frac{\beta(V + V_1 - V_{BE})}{R_b + R_e(1+\beta)}$

$\beta R_e >> R_b$; $I_C = \frac{V + V_1 - V_{BE}}{R_e}$

From the above equation, I_c is independent of β.

COMPENSATION TECHNIQUES

- Up to now, we have seen the techniques of stabilizing the operating point of the transistor which makes use of resistors in the biasing circuits.
- But in compensation technique, we use temperature sensitive devices like diodes, thermistors, sensistors etc.