MADE EASY

ELECTRICAL ENGINEERING

Digital Electronics

By.Ramesh Sir

- Theory
- Explanation
- Derivation
- Example
- Shortcuts
- Previous Years Question With Solution

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DIGITAL ELECTRONICS

Electronics: The study of motion of electron inside a semiconductor is known as electronics.

* semiconductors having controlled conductivity.
* for n-variables we get 2^n combination 2^{2^n} possible functions.

Boolean logic ideas:

These are classified into three parts –

1. Produce in the constant (0, 1)
   - 0 → null operation
   - 1 → identity operation.
2. Uniary operation (Buffer, not)
   - Buffer → transfer
   - not → complementary operation.
3. Binary operations (AND, OR, NAND, NOR, Ex-OR, Ex Nor, Inhibition, Implication)

Truth Tables

x	y	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

$f_0 = 0$ Null

$f_1 = x.y$ AND
$x \cap y$

$f_2 = x.\bar{y}$ Inhibition
(x but not y)

$f_3 = x$ transfer Buffer.

$f_4 = \bar{x}.y$ Inhibition
(y but not x)

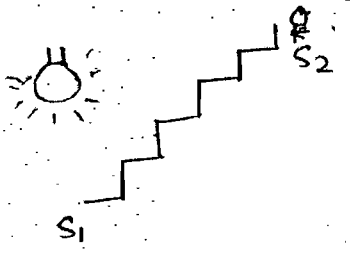
$f_5 = y$ Buffer (Transfer)

$f_6 = x \oplus y$ Ex-OR

$= \bar{x}y + x\bar{y}$

NOTE:

For. Staircase, a escalator Ex-OR logic is used.



S_2	S_1	$S_2 \oplus S_1$ bulb
0	0	0
0	1	1
1	0	1
1	1	0

$f_7 = x + y$ OR $x \cup y$

$f_8 = \overline{x+y}$ NOR $x \downarrow y$

$f_9 = x \odot y$ Ex-NOR $\bar{x}\bar{y} + xy$

NOTE: Ex-nor is also known as co-incidence logic, equivalence logic gate.

$f_{10} = \bar{y}$ NOT complimentary.

$f_{11} = x + \bar{y}$ Implication

$f_{12} = \bar{x}$ NOT Complimentary

$f_{13} = \bar{x} + y$ Implication

$f_{14} = \overline{x \cdot y}$ NAND
$x \uparrow y$

$f_{15} = 1$ Identity

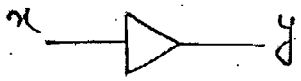
Basic logic gates : NOT, AND, OR.

Combinational logic gate :

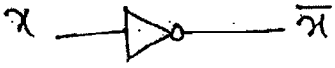
NAND, NOR } universal logic gate

Ex-OR, Ex-NOR } Arthmatic logic gate.

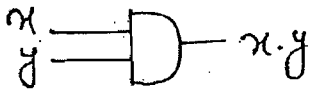
Symbols for logic gate



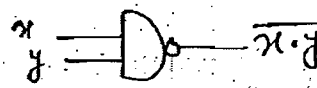
Buffer



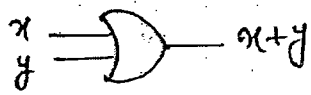
NOT



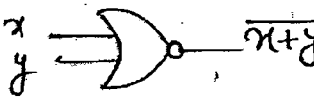
AND



NAND



OR



NOR.