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MADE EASY
ELECTRONICS ENGINEERING
ADVANCE ELECTRONICS
By-KAMESH Sir

- Theory
- Explanation
- Derivation
- Example
- Shortcuts
- Previous Years Question With Solution

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Advanced Electronics

1. VLSI Fabrication
2. VLSI Testing
3. VLSI Design

BOOKS: 1) S.K Gandhi.
2) S.M Sze.

Important source : Class Notes

Integrated Circuits :

Circuits : Combination (connection) of Active and Passive elements.

Active elements : BJT, MOSFET, JFET.

Passive elements : R, L, C

Integrated Circuit : Active and Passive elements are fabricated on a Substrate.

- Semiconductor.
- Insulator substrate.

IC	Discrete Circuits
1. Small size	1. Large size.
2. Low power consumption	2. High power consumption.
3. Low cost (due to Batch Process)	3. High Cost.
4. High speed.	4. Low speed.

eg: PCB (Printed ckt board)

Disadvantages of IC :

* Non Repairable only we can Replace IC.

Classification of IC's

- → Monolithic IC's
- → Thin / Thick film IC's
- → Hybrid IC's

Level of Integration
1. SSI
2. MSI
3. LSI
4. VLSI
5. ULSI

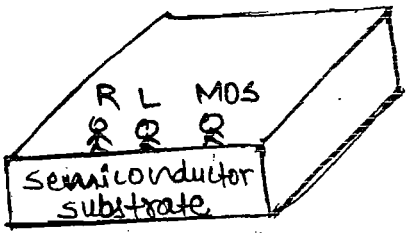
Analog IC's & Digital

Bipolar IC
CMOS IC
BICMOS IC

#Monolithic IC's :

Mono → single
lithic → stone.

In Monolithic IC's, complete ckt (active + passive element) are fabricated on a single substrate.



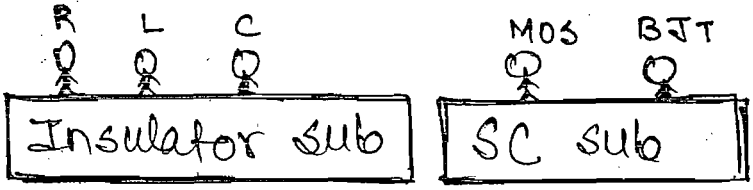
Disadvantage: Heavy value of R, L, C cannot be fabricated. Bcz heavy values of R, L, C required Large area of substrate.

Thin & Thick film IC's :

Thin & Thick film IC's looks very similar in appearance. Only difference is the method by which the conducting film is deposited on Insulator Substrate.

→ In this technology, the Active element are fabricated on Semiconductor substrate, whearase Passive elements are fabricated on Insulator substrate.

⇒ Heavy value of R, L, C are not restricted in this, compared to Monolithic IC's.



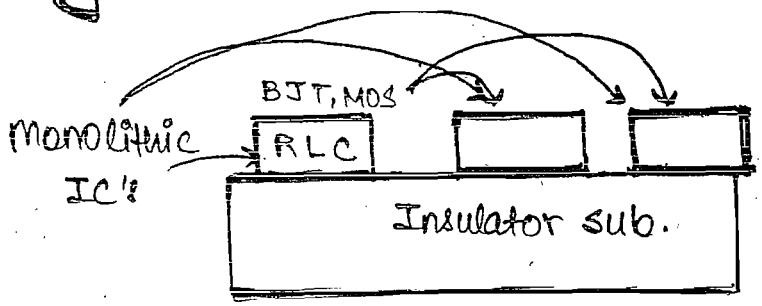
Thin film Technology

→ Conductive film is deposited by sputtering technique or by Vapour evaporation.

Thick film Technology.

→ Conductive film is deposited by screen printing or Silk screen printing.

Hybrid IC's :



Analog IC's : (Linear IC's)

Ex : IC-555, Op-amp 741.

I/P : Analog signal

O/P : Analog signal

Digital IC's : (Non-Linear IC's)

Ex: Flip-Flop

I/P → Digital signal
O/P → Digital signal

Level of Integration →

1. Small scale Integration (SSI) : 1-10 Tx per unit area
2. Medium " " (MSI) : 10-100
3. Large " " (LSI) : 100-10^4
4. Very Large scale Integration (VLSI) : 10^4-1M
5. Ultra Large scale Integration (ULSI)
   > 1M Tx per unit of the substrate.

- Packing density, $\boxed{P = \log_{10} Q}$

  Q: No. of Tx per unit area.

① SSI → (P < 1)
② MSI → (1 < P < 2)
③ LSI → (2 < P < 4)
④ VLSI → (4 < P < 6)
⑤ ULSI → (P > 6)

Bipolar IC's (BJT)

1. Low packing density
2. High gain.
3. High Bandwidth.
4. High Speed.
5. High power consumption.

CMOS IC's (NMOS PMOS)

1. High Packing density
2. Low gain.
3. Low Bandwidth.
4. Low speed.
5. Low power consumption

(2)

→ **Gain = g_m (Load)**

$g_m \longrightarrow$ Transconductance.

BJT:

$$g_m = \frac{I_c}{\eta V_T} = \frac{I_S e^{V_{BE}/\eta V_T}}{\eta V_T}$$

$V_{BE} \uparrow$, $I_c \uparrow$ exponentially, $g_m \uparrow$ exponentially.

MOSFET: $g_m = \sqrt{2 I_D \mu_n C_{ox} \left(\frac{W}{L}\right)}$

$I_D \propto (V_{GS} - V_T)^2$

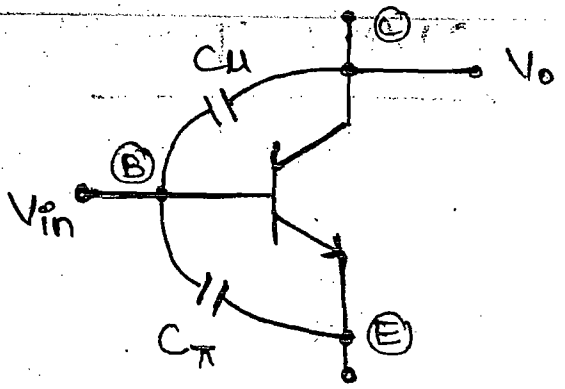
$V_{GS} \uparrow$, $I_D \uparrow$ (square law device), $g_m \uparrow$.

∴ **g_m (BJT) > g_m (MOS)**

Gain (BJT) > Gain (MOS)

* Collector is Lightly doped
* Base is moderately doped

③.



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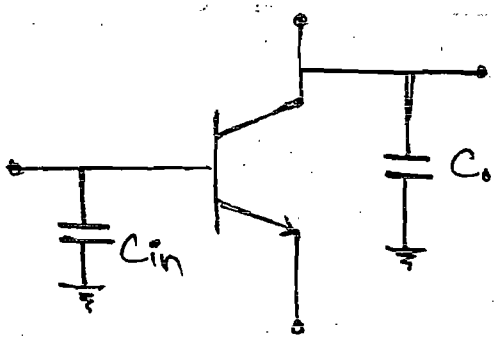
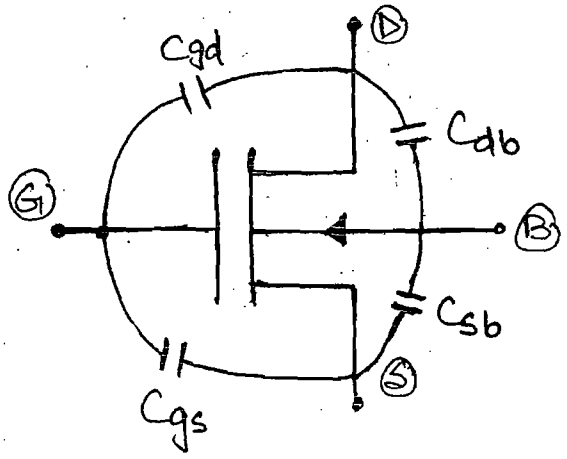


more capacitor, more delay.



$f_{H(MOS)} < f_{H(BJT)}$

* BW of (BJT) > BW of (MOS)

④. $t_r = \frac{0.35}{B.W}$
(rise time)

BW ↑ , t_r ↓

→ fast system.

∴ BJT is faster than CMOS.

#BiCMOS

→ When speed, gain is main concern then we prefer Bipolar IC's

→ When packing density and power consumption is main concern then we prefer CMOS ICs.