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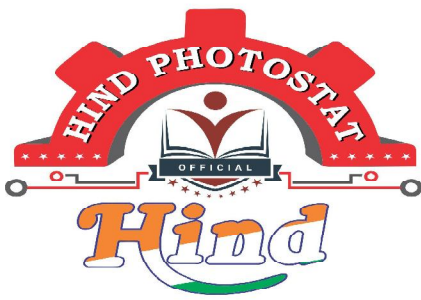
Computer Science Engineering / IT
Toppers Handwritten Notes

Digital Logic
By-Sriniwas sir

- Theory
- Explanation
- Derivation
- Example
- Shortcuts
- Previous Years Question With Solution

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DIGITAL LOGIC

[5-8 Marks]

Boolean Algebra

$r=2$ { Binary Number System }

(0, 1)

B. Variables $\Rightarrow A, B, C, \dots$

a, b, c, \dots

Operators $\Rightarrow \{OR, AND, NOT\}$

Algebra

$r=10$ { 0, 1, 2, ..., 9 }

SYLLABUS

(i) Boolean Algebra

- Boolean Variables
- Boolean Operators
 - Basic Operators { OR, AND, NOT }
 - Derived Operators { NAND, NOR, EX-OR, EX-NOR }
- Boolean Algebra Properties
- SOP, POS
- Universal Logic Gates
- Simplification of Boolean Expressions
or Boolean functions using properties
- Reducing K-Map or BF using minimum of NAND gates
or min. no. of NOR gates.
- EX-OR & EX-NOR Relations.

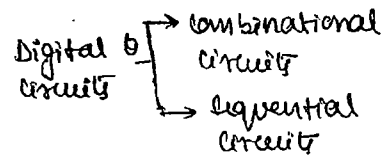
(ii) Number System:

- $()_{r1} = ()_{r2}$
- eg. $()_{10} = ()_8 = ()_2 = ()_4 = ()_6$
- $(r-1)$'s or r 's complement
- Signed Binary Number System
- Binary Numbers in Signed Binary No. System.

(iii) K-Map :

- Implicant, Prime implicant, Essential PI
- Dont care combinations
- Reading Minimal Expressions using K-Maps. (SOP or POS).

(iv) Combinational Circuits :



code converters \Rightarrow BCD to E3
 E-3 to BCD.

Binary to Gray code, etc.

Arithmetic Circuits \Rightarrow Half Adder, Full Adder
 Half Subtractor, Full Subtractor
 Binary Adder, Binary Subtractor
 BCD Adder, BCD Subtractor
 Magnitude Comparator
 Multiplexer, De multiplexer.
 Encoder, Decoder, Priority Encoder

(v) Sequential Circuits

- Binary Latch, Flip-Flops (FF)
- Conversions \Rightarrow FF1 \rightarrow FF2
 DFF \rightarrow J-K FF
 D FF \rightarrow T FF

- Registers
- Counters \rightarrow Asynchronous Counter (Asynchronous)
 Synchronous Counter (Synchronous)

Book:

Modern Digital Electronics
 - R.P. Jain

• Srinivas Bethi
 M. no. : 9959750099
 Mention : GATE 2024 Offline
 Student from Delhi

BOOLEAN ALGEBRA

Binary Operators: OR, AND

Basic operators: {AND, OR, NOT}

Unary Operator: NOT

(i) OR: $\Rightarrow +$, \cup , \vee

$$Y = A \cup B = A + B = A \vee B$$

$$Y = A + B + C + \dots$$

	A	B	A+B	AB
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	1	1

$$m=2 \Rightarrow 4$$

	A	B	C	A+B+C	ABC
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	1	0
4	1	0	0	1	0
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

$$m=8 \Rightarrow 8$$

Stmnt: The result of OR operation is zero if and only if all the variables are zero.

Truth Table:

n variables 2^n rows
 $\{0, 1, 2, \dots, (2^n - 1)\}$

Hardware components:

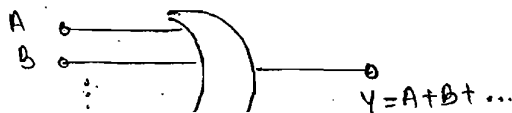
Logic gates

Integrated circuit (IC)

↳ Using PN Junction Diode

Transistors $\begin{cases} \rightarrow \text{BJT} \\ \rightarrow \text{MOSFET} \end{cases}$

OR GATE:



Logic gates are available for any no. of inputs.